Microlithographic Mask Development (MMD)

CDRL H007: Option 2 Contract Summary Report
CDRL H004: 4Q97 Contractor Progress, Status, Management Report

22 December 1997

Contract Number N00019-94-C-0035

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Administered by the Naval Air Systems Command

Lockheed Martin Federal Systems, Manassas, Virginia

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22 December 1997

ENCLOSURE NO: 97-MMD-LMFS-00092

Prepared for:

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Contract Number N00019-94-C-0035
Lockheed Martin Federal Systems

Lockheed Martin Federal Systems, Manassas, Virginia

Certification of Technical Data Conformity

The Contractor, Lockheed Martin Federal Systems, hereby certifies that to the best of its knowledge and belief, the technical data delivered herewith under Contract Number N00019-94-C-0035 is complete, accurate, and complies with all requirements of the contract.

Jan 5, 1998
Date

S.G. Schnur, Program Manager

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1.0 Introduction

This document, a combined Option 2 Contract Summary and Contractor Progress, Status, Management Report for 4Q97, is submitted in accordance with NAVAIR Contract N00019-94-C-0035, CDRL H007 and H004, respectively. The period from 25 November 1996 through 25 November 1997 is covered.

Program Summary

The primary goal throughout the Option 2 contract period was to eliminate the gold absorber process and implement a refractory metal process. With the initial transition completed, in which all mask patterning processes have been implemented within the MMD, the focus is currently on implementing all substrate fabrication steps within the MMD as well. This has resulted in the purchase and installation of some major equipment. In addition, our goal of developing processes for 130nm and below continues, and has also resulted in major equipment purchases and process changes. At the same time, we have been working on several important product demonstration masks for various customers.

MMD Contract Deliverables are shown in Figure 1 on page 4. The MMD schedule is shown in Table 1 on page 5.

Highlights

- A Leica LMS 2020 image placement metrology tool was fully qualified and implemented for production in January, 1997.
- Updated Validation Plan and Technology Roadmap documents were submitted during the first and second quarters of 1997 in accordance with contract requirements.
- The transition to a refractory metal absorber with SiC membranes was completed in March/April, 1997, and the gold process was eliminated.
- The installation of two additional pumps on the Suss Automated Resist Coating System to allow automatic dispense of multiple resist types was completed in June, 1997.
- A new, optimized resist process for SNR200 was implemented in June.
- UVIII resist was implemented for manufacturing and a Technology Acquisition Report was completed (reference CDRL G004, 97-MMD-LMFS-00076, 08 October 1997).
- The line monitor was transferred to 180nm NIGHTEAGLES from 250nm NIGHTHAWKS during April, 1997. Design was completed and the first masks were exposed for the 130nm line monitor, Viper.

- The modification to the KLA SEMSpec to accept single-mask SMIF pods was completed during September, 1997.
- Two new membrane hot plates were received and qualified in 3Q97.
- The acceptance test for the SSI Scorpio develop system was completed in September, 1997.
- Factory acceptance of a Sputtered Films Endeavor 8600 deposition system was completed and the tool has been installed in the MMD.
- An AG610 furnace on loan from IBM Yorktown has been installed and calibrated.
- A stress measurement system for the MMD was ordered in September, 1997.
- Ninety-five percent yield on image size was achieved during the IBM 1Gb (Phoenix) exercise. Sixteen masks were shipped, with critical areas defect-free; five of the 16 masks were refractory masks.
- Routine inspections for line monitors and products are now completed at 90nm sensitivity on the KLA SEMSpec.
- The Tencor 6420 Surface Inspection system has been fully qualified and released to production.
- An Energy Dispersive X-ray Analysis system was installed and qualified on the Amray AutoSEM.
- The KLA SEMSpec Array Mode Inspection software has been ordered and is due in December, 1997.
- An RFQ has been sent out for a particle inspection system to handle final mask substrates.
- One mask was successfully inspected at 70nm sensitivity on the KLA SEMSpec.
- New fluoroware boats and new mask boxes have been phased into the manufacturing line.
- All tooling modifications, with the exception of the Flatmaster warpage measurement system, have been completed in support of the 2.1mm thick wafer evaluation.
- An order has been placed for a fountain etch station.
- All current resist process tools have been successfully transferred to the new carbon/citric acid-filtered room, which was completed in October.
- All of the etch processes associated with the refractory metal absorber stack have been qualified.
- A Plasmatherm SLR730 PECVD System was purchased and installed. It is currently undergoing final process development prior to qualification into manufacturing.

- An order has been placed with Crystallume for 50 diamond films for evaluation of diamond as an alternate membrane material.
- Stress measurements of the SiC membrane and of SNR200 and UVIII resist before and after exposure were completed to provide inputs to the University of Wisconsin, Madison for modeling. Several models were run to simulate the refractory process steps.
- An evaluation of the new proximity algorithm was completed with current and simulated proximity patterns and was compared to the current algorithm.
- Positive tone 180nm line monitor Falcon was online in November, 1997.
- Product quality "MACH5" was shipped to the customer with one complete chip defect-free. Image placement measured 35nm.

0.25um PROTOTYPE

Qty=18, Not Defect Free, CD 3 sigma=40nm (goal=24), I/P=60nm (goal=36), CD mean=262-238

	D	J	F	M	A	M	J	J	A	S	O	N
Schedule	9*	9*										
Actual	9	9										

0.25um VALIDATED / DEFECT REDUCTION

Qty=16, Defect Free, CD 3 sigma=24nm (goal=20), I/P=36nm (goal=30), CD mean=262-238

	D	J	F	M	A	M	J	J	A	S	O	N
Schedule				1	1	1	2	2	2	2	2	3
Actual				1	1	1	2	2	2			

0.25um PRODUCTION

Qty=6, Defect Free, CD 3 sigma=20nm (goal=15), I/P=30nm (goal=23), CD mean=240-260

	D	J	F	M	A	M	J	J	A	S	O	N
Schedule										2	2	2
Actual										1		

0.18um PROTOTYPE

Qty=38, Not Defect Free, CD 3 sigma=30nm (goal=18), I/P=44nm (goal=20), CD mean=166-194

	D	J	F	M	A	M	J	J	A	S	O	N
Schedule	3*1*	3*1*	3	3	3	3	3	3	3	3	3	3
Actual	4	4	3	3	3	3	3	3	3	2		

0.13um PROTOTYPE

Qty=5, Not Defect Free, CD 3 sigma=20nm (goal=12), I/P=30nm (goal=18), CD mean=120-140
(Early learning masks, spec applies for 1998 only)

	D	J	F	M	A	M	J	J	A	S	O	N
Schedule			1			1			1		1	1
Actual			1			1			1		1	1

**Left over from option year #1 contract deliveries*

Figure 1. MMD Contract Deliverables (December, 1996 - November, 1997)

Table 1. 1997 MMD Objectives

	1Q97	2Q97	3Q97	4Q97
Line Monitor	*0.18μm Au product* *10 defects/cm² @ 90* *5 starts/wk* *IP=35nm,CD=20nm*	*0.18μm Ref Proto* *Defects: N/A* *5 starts/wk* *IP=50nm,CD=25nm*	*0.18μm Ref Proto* *Defects: N/A* *5 starts/wk* *IP=40nm,CD=22nm*	*0.18μm Ref Proto* *Defects: TBD* *5 starts/wk* *IP=30nm,CD=18nm*
Product Applications	*6MGb SRAM test site* *1Gb DRAM test site* *PXLA Product Masks*	*64Mb SRAM test site* *1Gb DRAM test site* *PXLA Product Masks*	*64Mb SRAM test site* *256Mb SRAM t/s* *IBM Logic test mask* *PXLA Product Masks*	*64Mb SRAM test site* *256Mb SRAM t/s* *IBM Logic test mask* *PXLA Product Masks*
MMD Contract Deliveries	*0.25μm/0.18μm/* *0.13μm masks*	*0.25μm/0.18μm/* *0.13μm masks*	*0.25μm/0.18μm/* *0.13μm masks*	*0.25μm/0.18μm/* *0.13μm masks*
		Technology Learning		
	TaSi etch development	**Complete transition to refractory metal absorber for POR**	**Radiation damage tests with full refractory stack**	*Absorber deposition system qualification*
	Tencor 6420 acceptance test	**Order fountain-cup etch station**	**SSI Develop tool acceptance test**	*XEP0 laser and magnetics upgrade*
	SiON etch process transfer to MMD	**Order absorber deposition system**	**Install EDX on AutoSEM**	*KLA array mode software installation*
	Implementation of P5 post-processor	**Installation of SiON deposition system**	**KLA Single SMIF upgrade**	**4Gb DRAM (0.13μm) test site design/build**
	SiON deposition system acceptance test	**Order P0 upgrades (DACs, laser, and magnetics)**	**Interim anneal furnace ready for process**	*Fountain-cup etch system acceptance test*
		Order film stress measurement system	*Install XEP0 14Gbit DACs*	*Stress measurement system qualification*
		Characterize defects and identify sources	**Build new carbon/ citric filter room**	*Order thickness measurement system*
		UVIII resist process qualification		*Order anneal system with integrated SMIF*

Note: Highlighted text indicates completed activity.

2.0 Validation Study (Task 1)

Task Objective: ***Develop a pilot line validation study for the production of masks with test and/or circuit patterns that use 0.25μm and 0.18μm design rules.***

2.1 Validation Plan

The Validation Plan, CDRL G001, was updated on 28 February 1997 (reference 97-MMD-LMFS-00018) and on 23 May 1997 (reference 97-MMD-LMFS-00042) in accordance with contract requirements.

2.2 NIGHTEAGLE Manufacturing Measurement Vehicle

2.2.1 NIGHTEAGLE Writes per Plan

The number of NIGHTEAGLE writes per plan are shown in Figure 2. Two significant changes were made during the contract period, both of which were completed in April: 1) line monitors were exclusively 0.18μm NIGHTEAGLES and Falcons, and 2) the transition to the refractory mask process was completed. Line monitor exposures were limited by substrate availability, as Hoya SiC masks were divided among product requirements, process development and line monitors. Beginning in mid-July, a target of three exposures per week was attempted with moderate success. Work is underway to expose the the 0.13μm Viper during the fourth quarter of 1997.

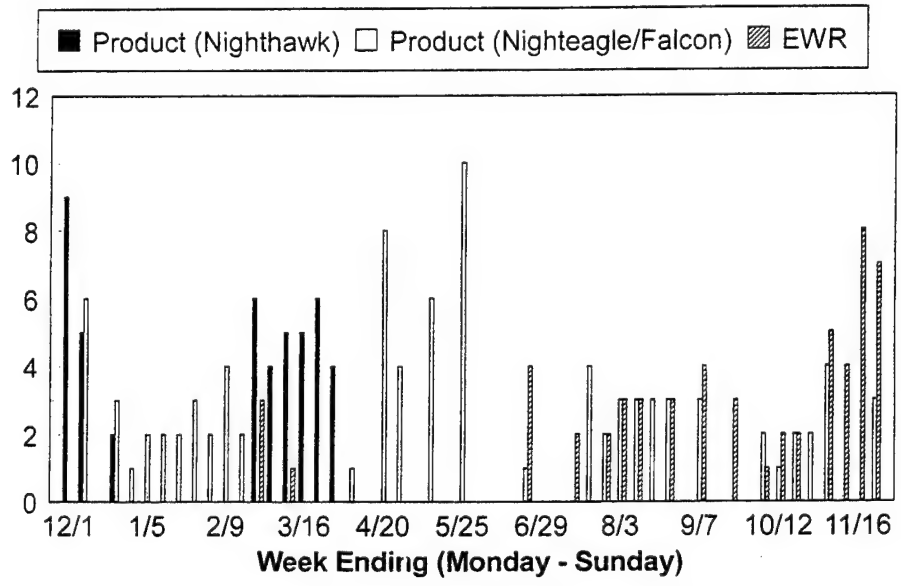


Figure 2. Line Monitor Writes per Week

2.2.2 NIGHTEAGLE Yields

Yields for NIGHTEAGLE masks were measured for overall yield and for the individual yields of image size, image placement, and defects. Figure 3 on page 7 shows all the yields. The targets for each yield are 80%, 80% and 25% for image size, image placement and defects, respectively. The overall yield target is 16%.

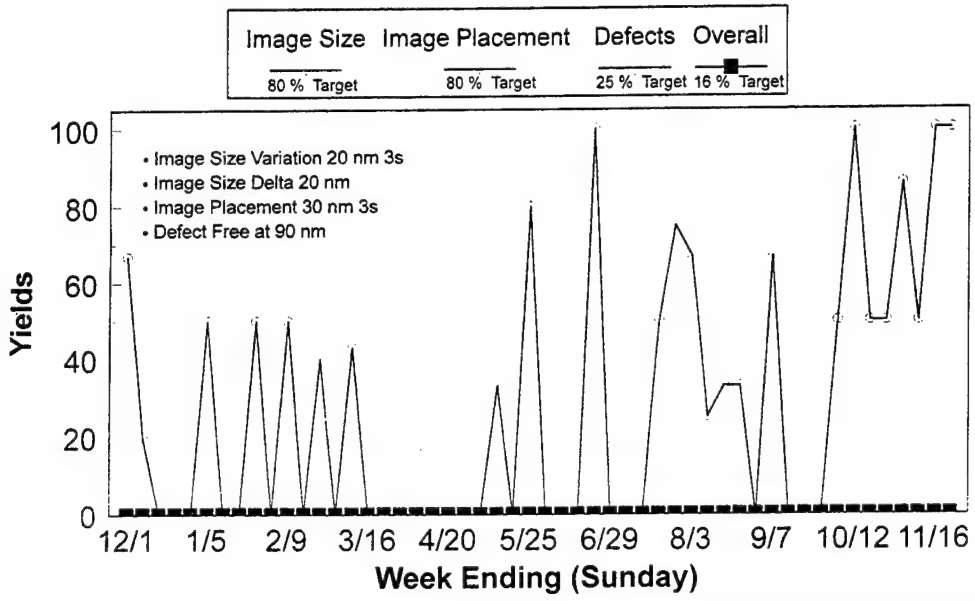


Figure 3. Line Monitor Yield

2.2.3 Image Size

Image size results for line monitor masks are shown in Figure 4 on page 8. Image size performance has been mixed. Line monitor performance has yielded a part at 9nm, the lowest 3σ variation seen on line monitor, but has also shown unacceptable part-to-part variation ranging as high as 35nm. Some of this variation can be attributed to etch process development, which is ongoing. In addition, a significant effort has been made to understand the effects of post-expose resist bake. In the fourth quarter, experiments were designed to determine the contribution of e-beam fogging with UVIII and SNR200. It is expected that all these factors contribute to the image size variation seen, and it will be a major task in 1998 to understand and reduce these effects.

Despite these mixed results on the line monitor, performance on critical image disposition on customer masks has been excellent. There was a 95% yield on image size on the 20nm specification for the IBM 1Gb (Phoenix) test mask exercise, with best performance being 6nm. Similar results have been seen on current IBM and Motorola orders.

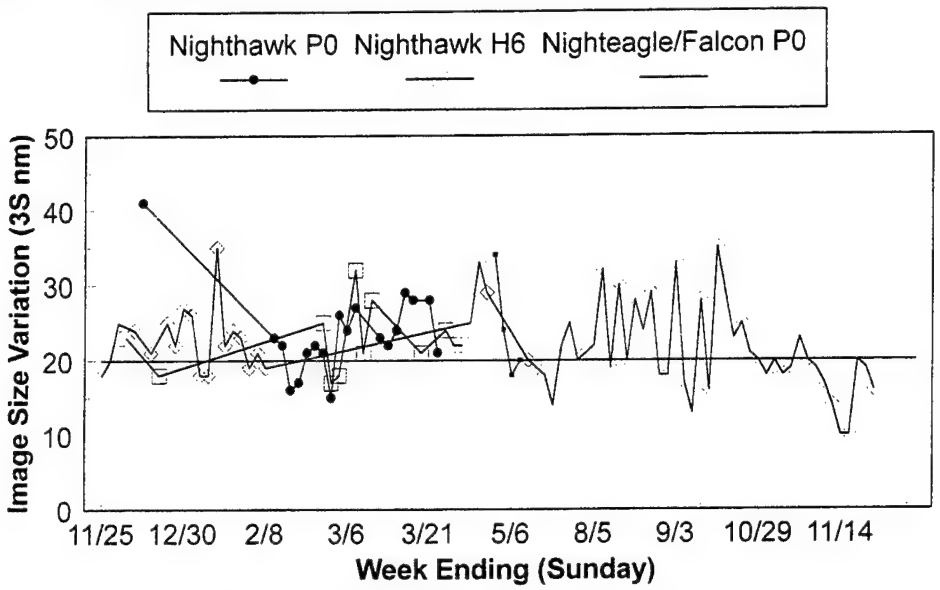


Figure 4. Image Size Variation (Line Monitor)

2.2.4 Image Placement

Image placement results for line monitors are shown in Figure 5. Image size results on the NIGHTEAGLE line monitor have been disappointing. At the start of the contract period, NIGHTHAWK and NIGHTEAGLE gold masks exposed at EL-4 P0 were single-pass exposed due to a charging problem. Single-pass exposure results in an approximately 50% increase in image placement performance. Initial refractory mask learning precluded the down-time needed to fix this problem. Frequent Product Specific Emulation (PSE) updates were required to keep image placement below 50nm. Charging problems were minimized in the middle of the contract year.

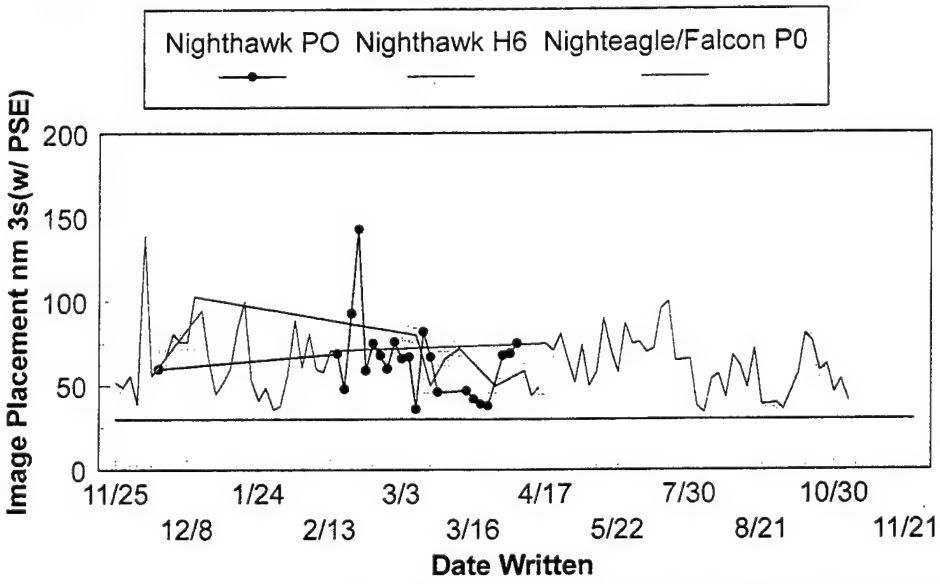


Figure 5. Image Placement (Line Monitor)

During the third quarter, the line monitor became exclusively refractory NIGHTEAGLE. Initial PSE attempts were not successful due to process development changes and stress issues with the deposited stack. It was found that a PSE created with one particular lot would give 30-40nm placement within that lot, but >50nm with the next lot. The new deposition tool, which is currently being qualified, is expected to provide better stress control.

Image placement results on customer masks have been promising. Several masks from the IBM 1Gb (Phoenix) exercise were <35nm, with the M0 level yielding 50% at 35nm with a best performance of 28nm. Image placement of less than 40nm has been obtained on NIGHTHAWK, NIGHTEAGLE, four levels of the IBM 1Gb test mask, and MACH5 (IBM logic microprocessor with 0.25μm groundrules) during 1997.

2.2.5 Defect Learning

The defect learning for line monitors is shown in Figure 6. Defect learning on refractory masks progressed very well during the contract period. Line monitor performance decreased from >500 defects/cm^2 down to <10 defects/cm^2. This includes the reduction of KLA SEMSpec sensitivity from 120nm to 90nm. Nonrepairable defects in the silicon carbide substrates prevented defect-free line monitors from being fabricated during the year. The MMD is working closely with Hoya to eliminate SiC nonrepairable defects.

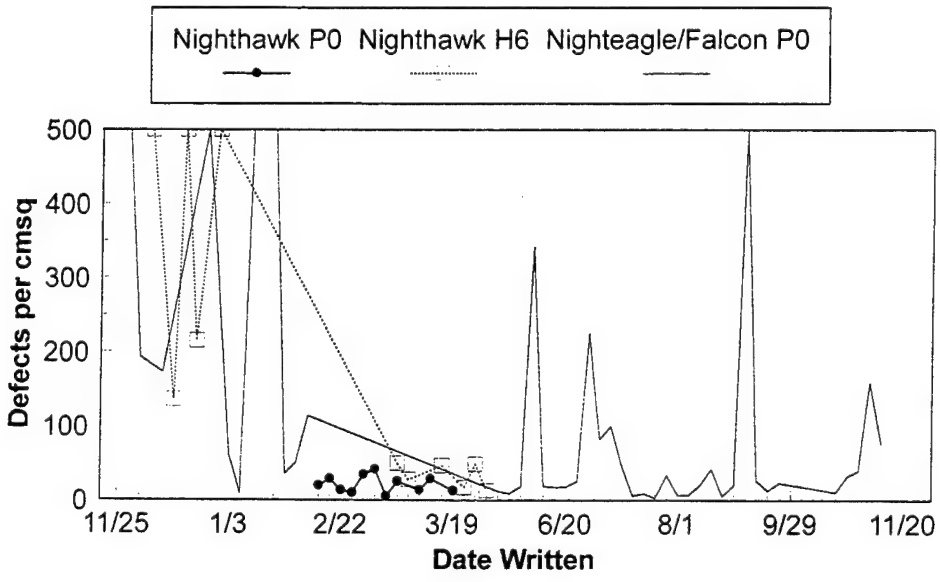


Figure 6. Defect Density (Line Monitor)

Customer mask performance was excellent. Sixteen masks were shipped defect-free in the critical areas; five of these shipments were refractory masks. In November, 1997 a full, defect-free chip on the MACH5 was shipped to the customer.

3.0 Roadmap Activities (Task 1)

Task Objective: ***Devise a comprehensive MMD technology roadmap.***

3.1 Technology Roadmap

The Technology Roadmap (CDRL G002) was updated on 11 March 1997 (reference 97-MMD-LMFS-00019) and on 20 May 1997 (reference 97-MMD-LMFS-00043) in accordance with contract requirements.

3.2 Metrology and Inspection

3.2.1 Tencor Surface Inspection System

The MMD requires a surface inspection system with higher defect sensitivity. A market survey was performed in late 1996 and the decision was made to purchase the Tencor 6420 Surfscan system. The system has been fully qualified and released to production. The system sensitivity data for the various inspection films is shown in Table 2. The overall project schedule is shown in Figure 7 on page 11.

Table 2. System Sensitivity, Membrane-Wafer System

Substrate	Sensitivity Source Acceptance (μm)
Si Wafer	*0.100*
B-Si Wafer*	*0.241*
B-Si Membrane	*0.241*
SiC-Coated Wafer	*0.236*
SiC Membrane	*0.238*
TaSi (Refractory)	*0.238*
TaSi w/ SiON (Refractory)	*0.238*
Final Mask Gag Inspection	*5.000*

* Boron-doped silicon

3.2.2 Energy Dispersive X-Ray Analysis System

An energy dispersive x-ray analysis system, the Oxford Link ISIS Series 300 Microanalysis System, was purchased to support defect reduction work. The system was installed and qualified on the Amray AutoSEM, and will allow for elemental analysis of defects found on the Tencor Surfscan 6420 and the KLA SEMSpec.

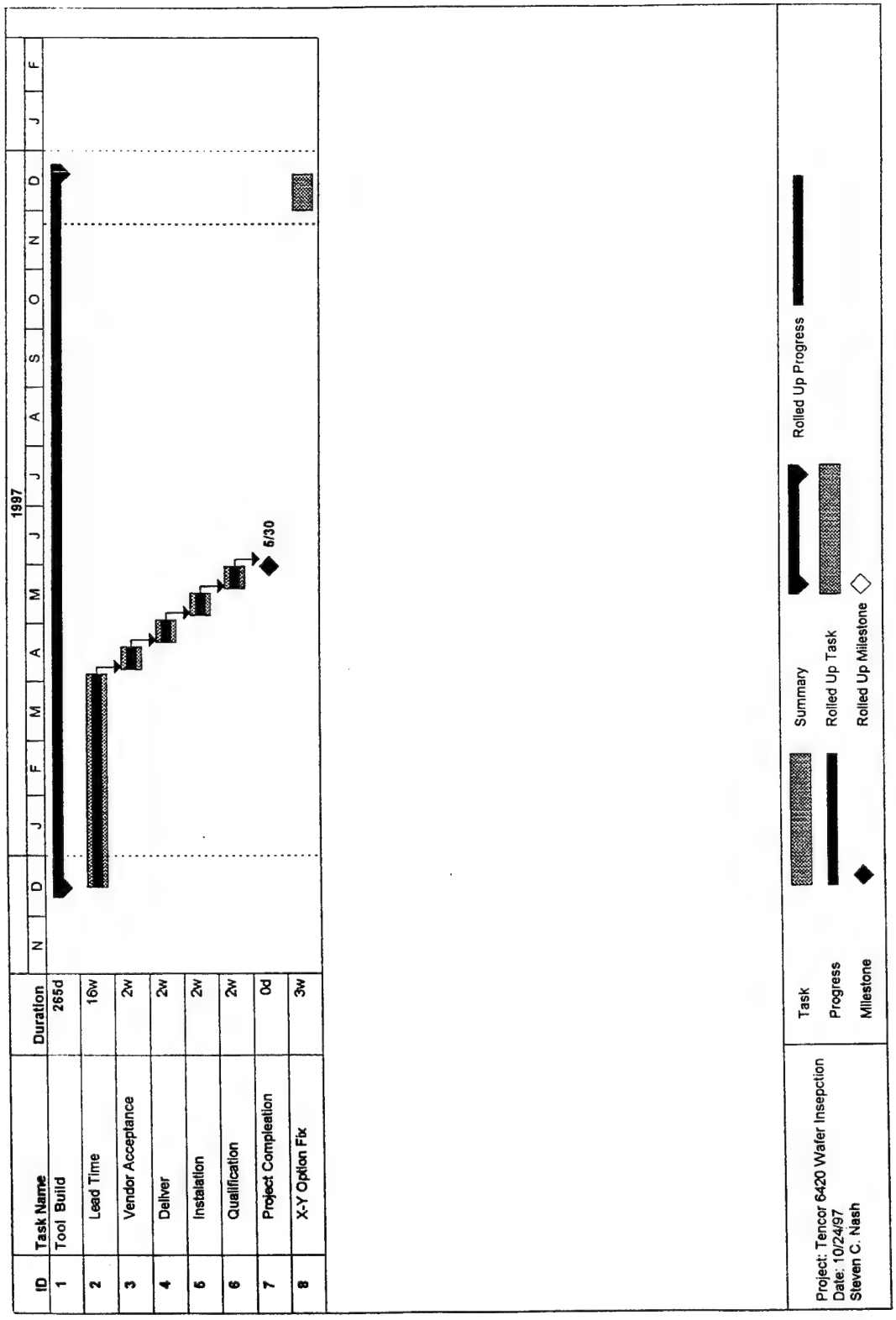


Figure 7. Tencor 6420 Surface Inspection System

3.2.3 Thin Film Stress Measurement System

Film stress is important for image placement control. A thin film stress measurement system is needed in the MMD to control the stress level in the TaSi and SiON deposition process. A Tencor FLX 4500 in the IBM Burlington manufacturing line was available for use while MMD evaluated the Tencor and the FSM stress tools. Based on the evaluations, a decision was made to purchase the Tencor FLX 5510 system which will undergo source acceptance during January, 1998. The overall schedule is shown in Figure 8 on page 13. Acceptance criteria is the system signal-to-noise. The expected system minimum detectable stress levels for the various films are listed Table 3.

Table 3. System Resolution

Film Type	Average Stress *	Stress Uniformity **	Phantom Film Thickness (Å)
Si	±2.5	8	5000
TaSi	±2.5	8	5000
SiON	±6.0	15	2000
Cr	±40.0	120	200

* For the average stress the system resolution (1s) will be less than (MPa)
**For the stress uniformity (1s) the system resolution will be less than (MPa)

The Tencor system will have integrated SMIF input/output with a class 1 mini-environment. The software is also being modified to support MMD requirements.

3.2.4 KLA SEMSpec Array Mode Inspection

Proximity X-Ray Lithography Association (PXLRA) funding was released in 1997 for purchase of the array mode inspection software option for the KLA SEMSpec. Delivery is scheduled for December, 1997, and the system is expected to be on line 15 January, 1998. The project schedule is shown in Figure 9 on page 15. The array mode inspection is specifically designed to inspect masks with repetitive patterns (e.g., DRAM and SRAM cells). The defect detection mechanism of array mode inspection is based on a cell-to-cell comparison (versus die-to-die mode with the current software). The defect detection algorithm looks for differences between two adjacent cells (within microns of each other) and flags a detected difference as a defect. An arbitration algorithm will be used to determine where the defect is located. There are several advantages and disadvantages in running inspection in array mode. One advantage is that by comparing images over such a short distance, the system will not be as sensitive to image placement errors and to systematic image size errors. In addition, inspection of single die masks can be performed in the array area It may also be possible to obtain higher sensitivity inspections. The major disadvantage of array mode is that only the repetitive pattern areas within a die will be inspected. As stated above, this limits the application to memory devices.

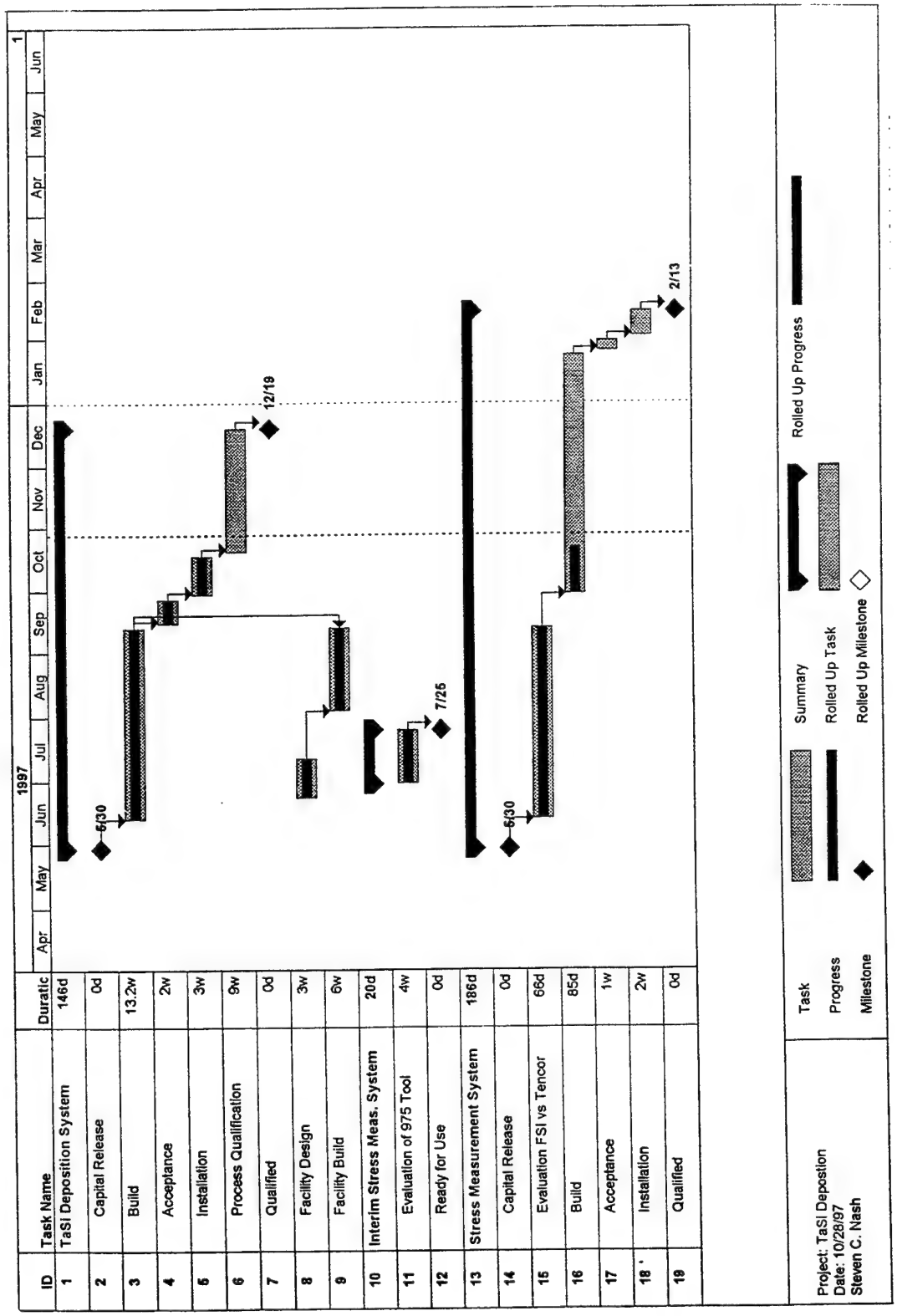


Figure 8 (Part 1 of 2). TaSi Deposition Project Schedule

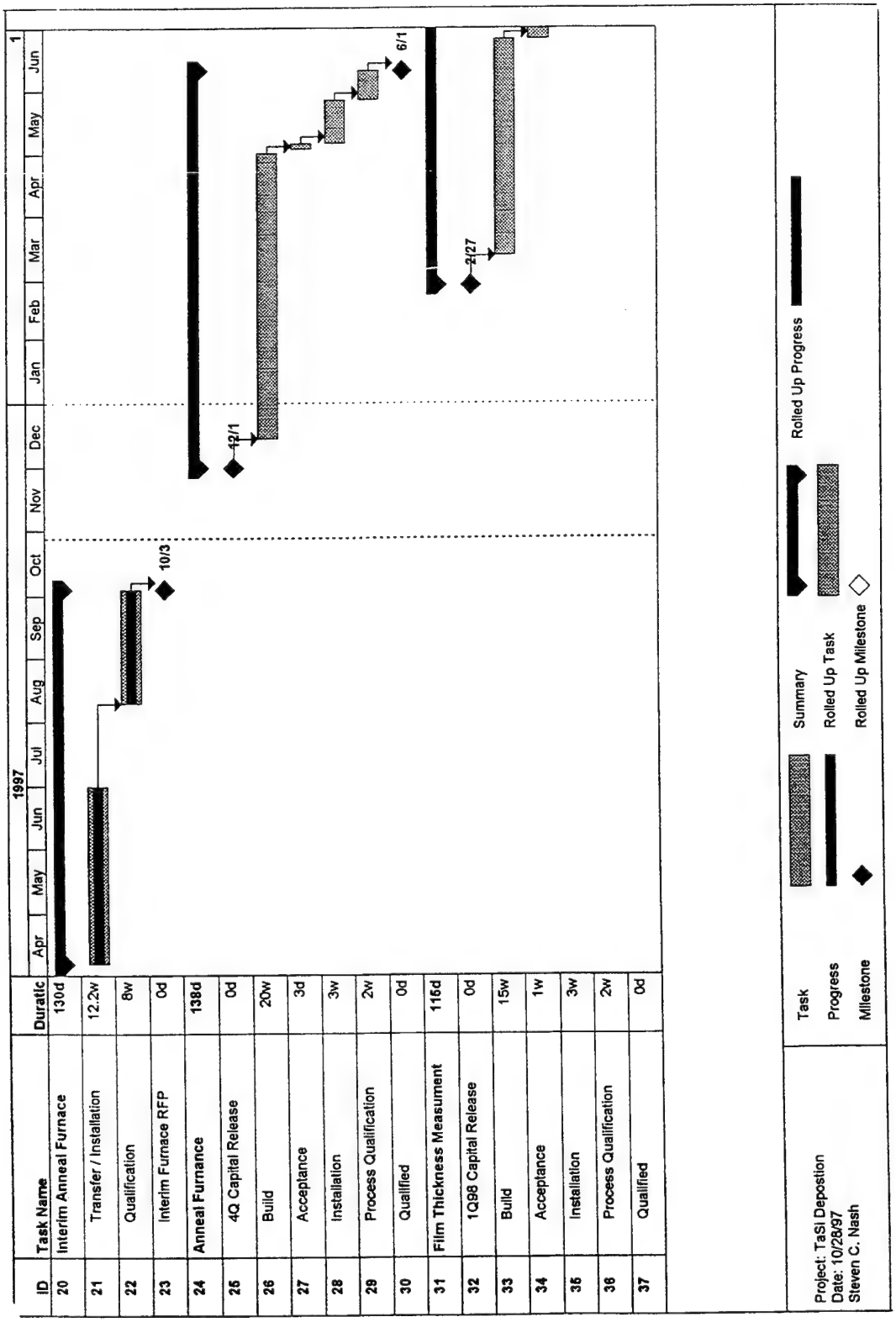


Figure 8 (Part 2 of 2). TaSi Deposition Project Schedule

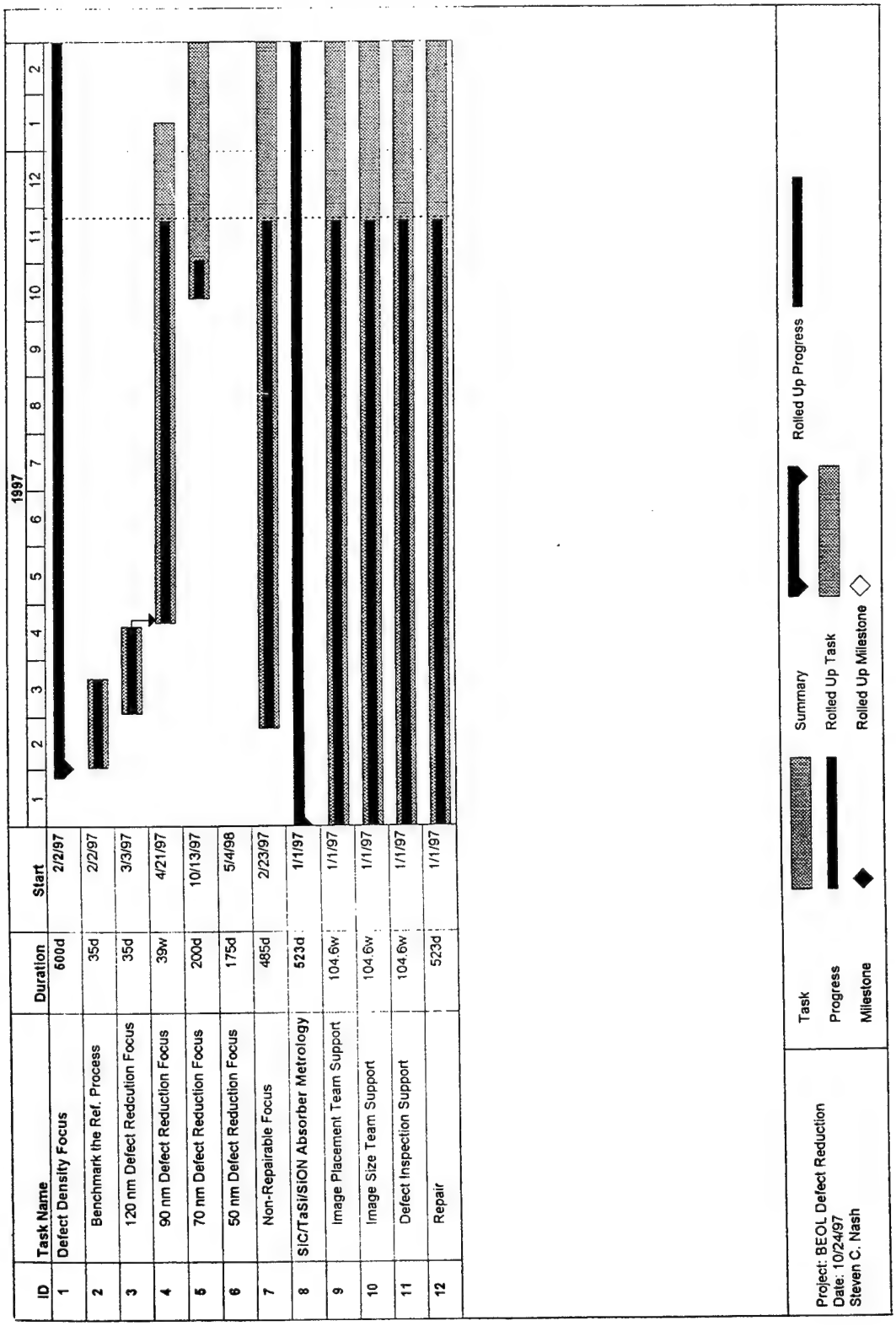


Figure 9 (Part 1 of 5). Defect Reduction Project

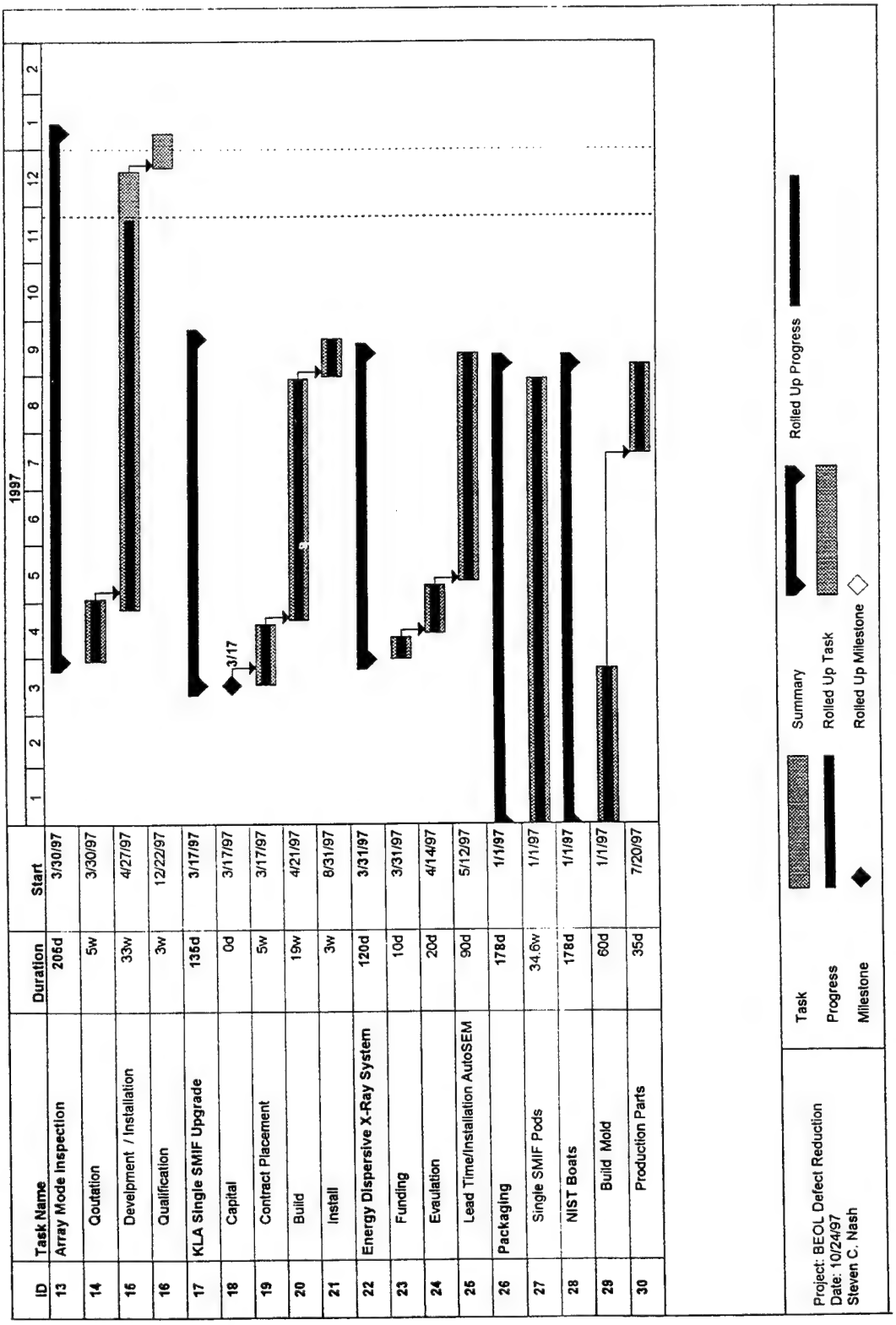


Figure 9 (Part 2 of 3). Defect Reduction Project

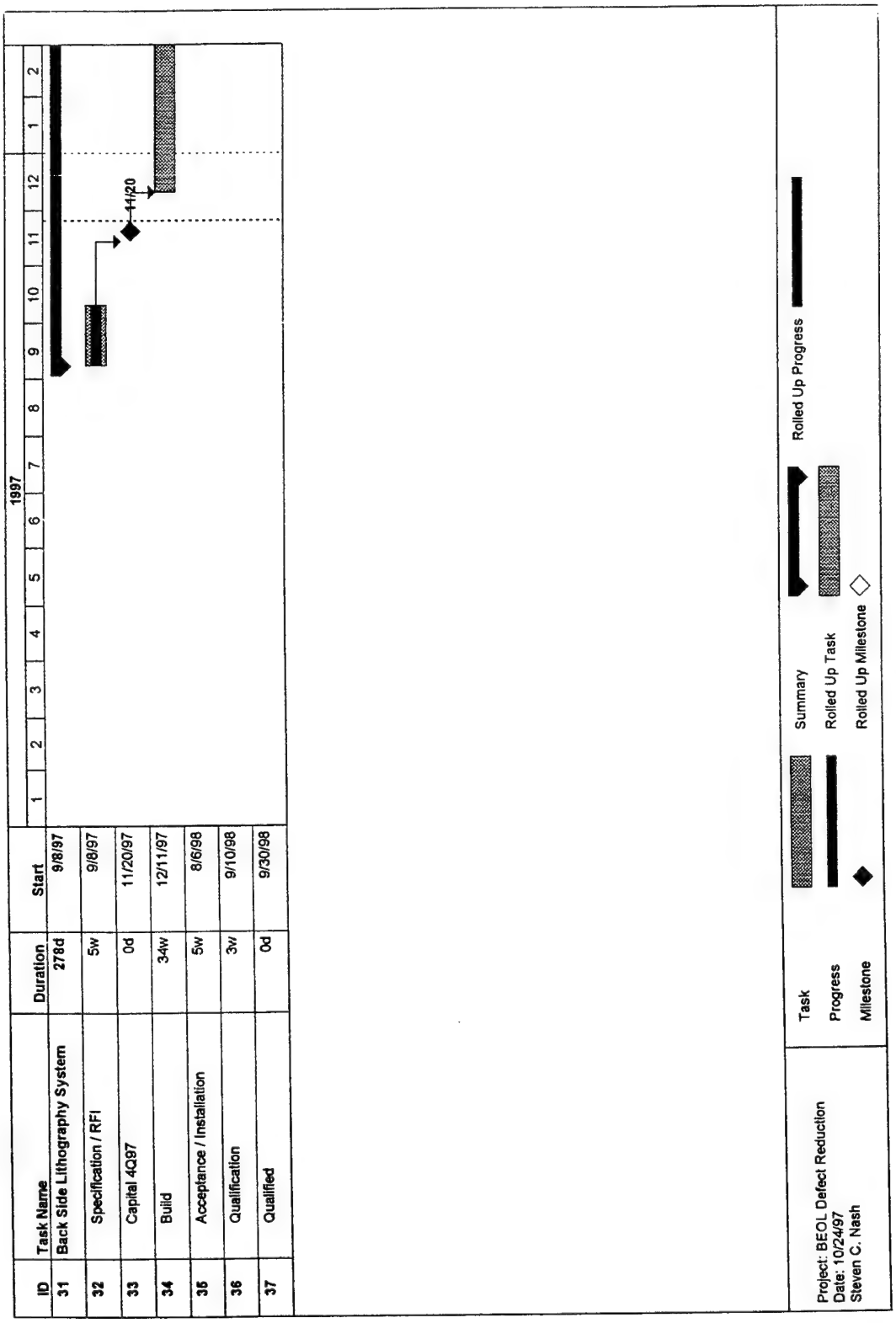


Figure 9 (Part 3 of 5). Defect Reduction Project

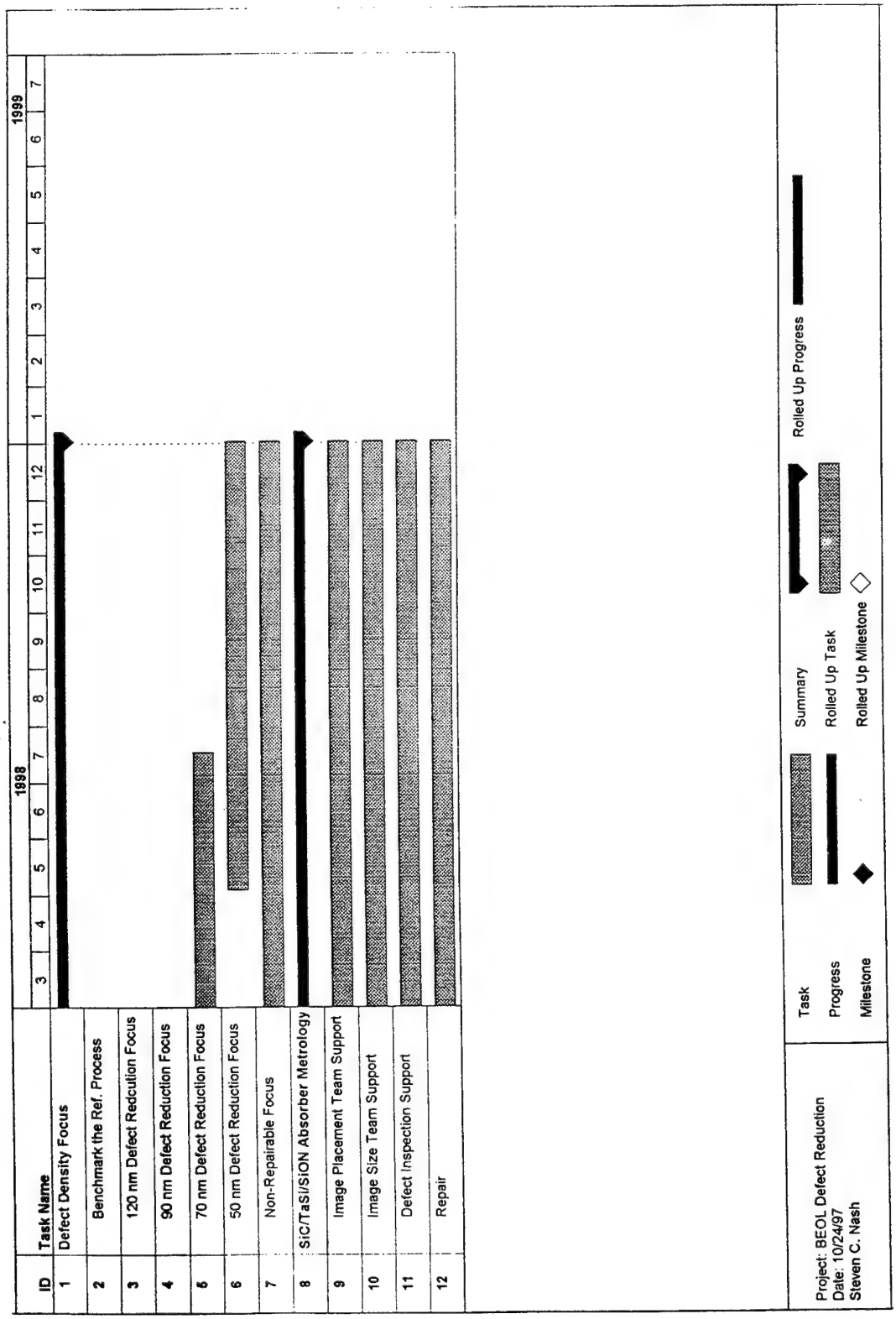


Figure 9 (Part 4 of 5). Defect Reduction Project

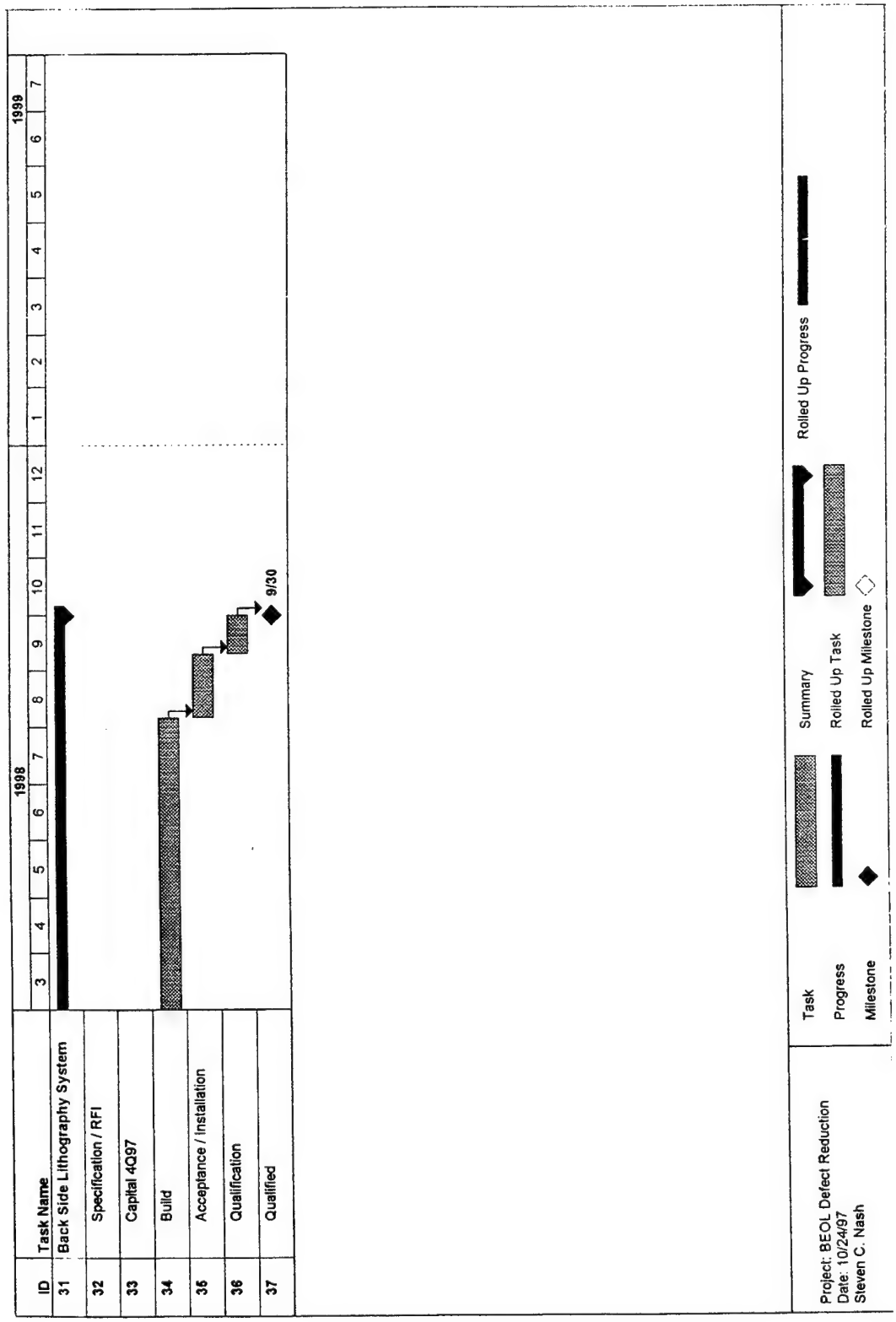


Figure 9 (Part 5 of 5). Defect Reduction Project

3.2.5 Substrate Defect Inspection System

The Q.C. Optics defect inspection system used to inspect x-ray mask substrates in the MMD must be replaced. The current Q.C. Optics system sensitivity is higher than 3μm on the TaSi/SiON films stack. A specification of requirements has been sent to Inspex, Q.C. Optics, KLA-Tencor, Eutecnics, and Applied-Orbot; quotations are expected back by mid-December, 1997, at which time an evaluation will be done to determine the best candidate. The project schedule is shown in Figure 10 on page 21. The requested system sensitivity is shown in Table 4.

The film stack that is to be inspected is shown in Figure 11 on page 23.

Table 4. System Sensitivity X-Ray Mask Substrates

Substrate	Sensitivity (μm)
TaSi	*0.150*
TaSi with SiON	*0.150*
TaSi with Cr	*0.150*
TaSi/SiON with Resist	*0.150*

3.2.6 Analytical SEM

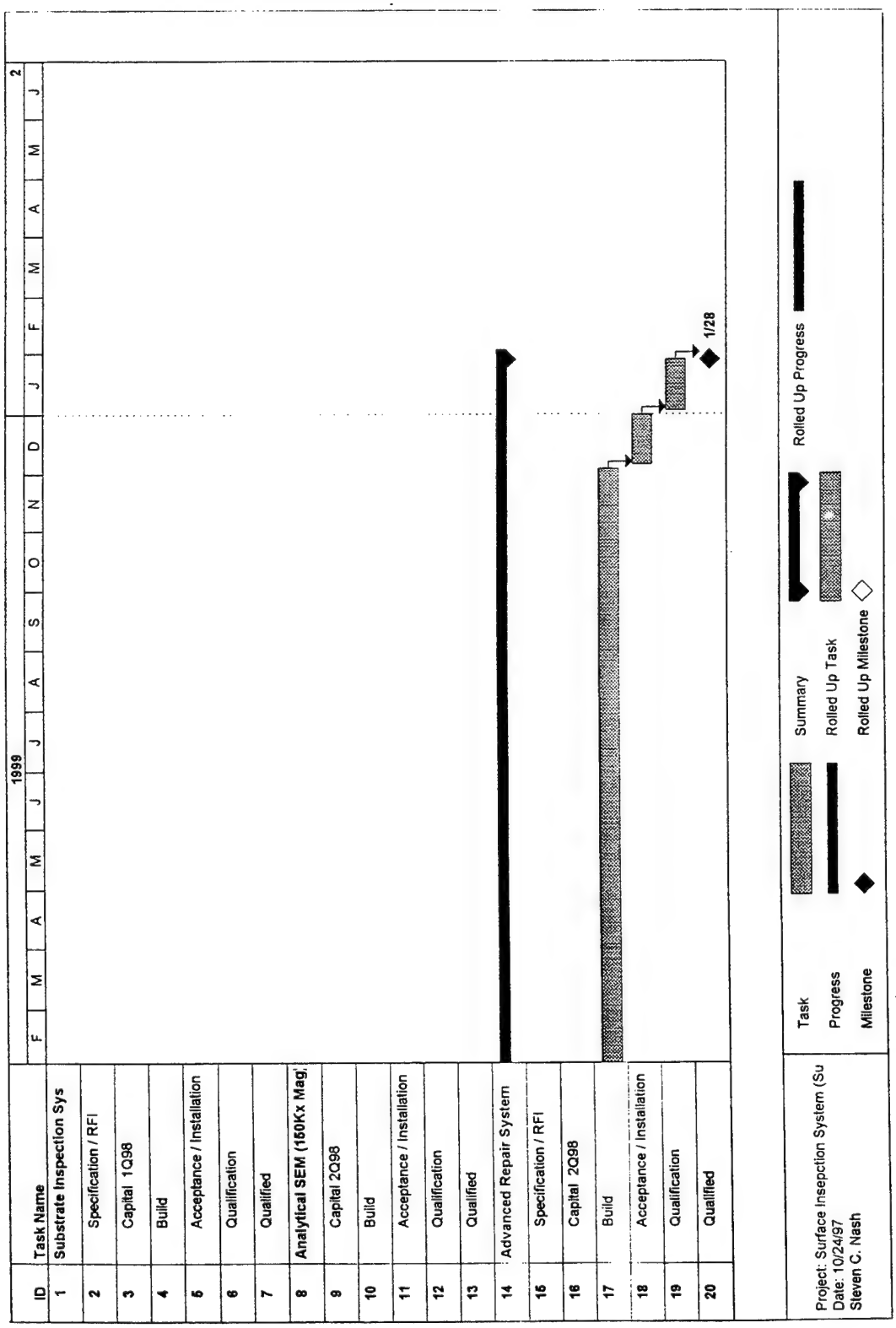
The MMD requires a higher resolution scanning electron microscope to support the development of 0.100μm groundrule masks, and plans to purchase a new analytical SEM in 1998. The project schedule is shown in Figure 10 on page 21.

3.2.7 KLA SEMSpec Adapter Change

A new adapter for the KLA SEMSpec is required to support the inspection of the new SFI films. The SFI system leaves a 2mm ring around the mask that has no metal (Cr/TaSi) deposited on it. In order to achieve proper grounding, the adapter for the KLA SEMSpec must be redesigned to move the grounding points further in. A new adapter has been ordered.

3.2.8 Leica LMS 2020 Trade-in

A Leica LMS 2020 image placement metrology tool was fully qualified in January 1997, and has been handling MMD production since that time.



ID	Task Name
1	Substrate Inspection Sys
2	Specification / RFI
3	Capital 1Q98
4	Build
5	Acceptance / Installation
6	Qualification
7	Qualified
8	Analytical SEM (160Kx Mag)
9	Capital 2Q98
10	Build
11	Acceptance / Installation
12	Qualification
13	Qualified
14	Advanced Repair System
15	Specification / RFI
16	Capital 2Q98
17	Build
18	Acceptance / Installation
19	Qualification
20	Qualified

Figure 10 (Part 1 of 2). Substrate Inspection System and Metrology Equipment

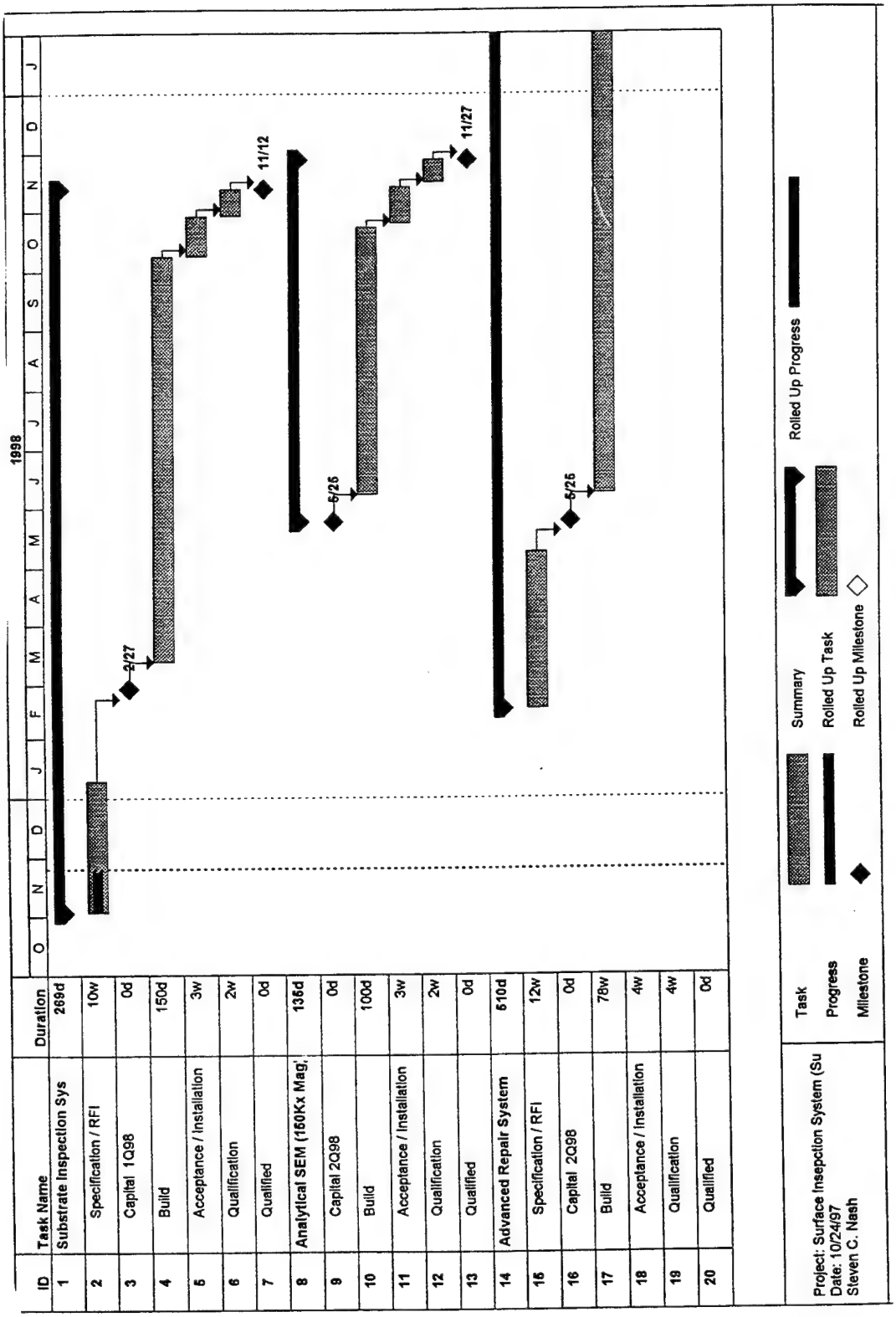


Figure 10 (Part 2 of 2). Substrate Inspection System and Metrology Equipment

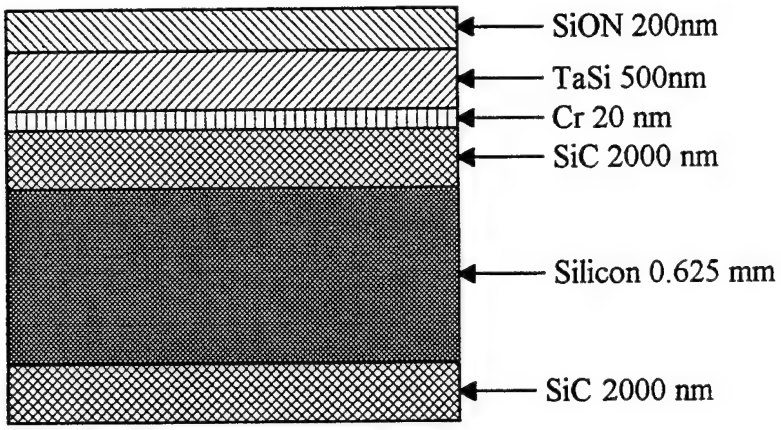


Figure 11. Film Thickness - Ta with SiON

3.3 Process Equipment

3.3.1 Suss Automated Resist Coating System, Tool Status

Due to corrosion, possibly caused by exposure to acid at the Suss factory, the robot end-effector on the Suss coater was replaced on 12 March 1997.

Maintenance training classes were held in April and the internal maintenance group was satisfied with the course.

The installation and software integration of the two additional Millipore resist pumps was completed in early June. The UVIII resist pump was operational and implemented for product on 6 June 1997.

The SJR (FEOL) pump, which had been used successfully with solvent, would not pump SJR resist due to its high viscosity. The resist would not pass through a filter, but the pump required a filter. On Millipore's suggestion, a stealth filter, which is a filter without a membrane, was installed on the pump and the process was implemented for all FEOL product in July.

Corrosion on the pre-aligner for the Suss coater was noticed during laser maintenance in August. Suss determined that the protective coating was removed during machining (a hole was cut in the center of this component after the coating process). The supplier is building a replacement part for the Suss tool.

3.3.2 New Automated Develop Tool

The SSI develop/bake cluster tool consists of a SMIF load station, robot, prealigner, three hot plates, a chill plate and a develop module with two develop pumps (capability for two developer types). The source acceptance test was completed in Freemont, California on 5 November 1997. The tool arrived in the MMD facility on 12 November and is presently being installed in the new carbon/citric filtered room. The tool qualification will be completed during 1Q98.

3.3.3 New Carbon/Citric Filtered Room

The new carbon room was ready for equipment (RFE) on 10 October 1997. The equipment move started on 13 October and was completed on 22 October. The tool setup/requalification was completed and the resist apply process was back on-line for product on 24 October 1997.

3.3.4 New Hot Plate

Two new CE1100 Brewer membrane hot plates were received and qualified in 3Q97. The new hot plates have a vacuum style pedestal as opposed to the original screw on type which created a FM problem. The original wafer hot plate has been converted to a vacuum style hot plate which can be used for wafers, bonded wafers and bonded membranes.

4.0 Develop 0.25μm Mask Fabrication Capability (Task 3)

4.1 0.25μm Defect Reduction/Validated Mask Fabrication (Task 3.2)

Task Objective: Establish and maintain a pilot production facility capable of on-premises x-ray mask production, and demonstrate 0.25μm mask fabrication capability by fabricating masks of increasing complexity.

4.1.1 Line Status

The major accomplishment during this contract period was the implementation of the refractory mask process and the elimination of the gold process. This was completed by the end of the first quarter of 1997, three months ahead of schedule.

Completion of the IBM 1Gb test mask order was a significant highlight in 1997 with regard to line performance. Five levels were shipped with backups and included 16 defect-free masks. Three of the levels were made with gold absorber and two were made with the new refractory process. Also, a complete, defect-free MACH5 chip was shipped to the customer Image placement was 35nm and image size was 3σ <20nm, exceeding customer specifications. Currently, line loading with refractory masks is approaching the levels previously seen with gold masks. Work is underway to do image size learning (bake, new develop tool, fogging, etc.), image placement learning (film stress control, multipass writing) and defect control (SiC substrates, FM). There are currently six mask orders in the line (three IBM, and one each for Sanders (a Lockheed company), University of Wisconsin and Motorola) along with the 0.13μm and the 0.18μm line monitors.

EL-4 P0 had excellent availability, especially in the second half of the year. Charging problems seen during the first quarter were reduced in the second quarter, and heated second and fourth aperture assemblies were installed to improve aperture lifetime. The KLA SEMSpec reduced sensitivity from 120nm to 90nm during the year, with defect performance on refractory masks ahead of schedule. The plan is to reduce to 60nm sensitivity in 1998. The RIE etch process was transferred from PCRL Motorola during the first half of 1997. The new Plasmatherm etch system was qualified and the transferred process was optimized for SNR200 masks; it is currently being optimized for UVIII masks. In addition, the new Leica 2020 image placement system was installed and qualified in the MMD.

4.1.2 Equipment Engineering Changes and Facilities Activities

Suss Resist Coat Tools

- Two additional Millipore resist pumps were installed and tested. Total resist capacity is now four. The two additional pumps will be used for the FEOL resist and UVIII positive resist.

- A NOWPAK resist dispense system was installed for new conductive resist experiments on the small Suss coater.
- A digital scale for the resist bottle was installed to indicate proper replacement cycles. This improves process performance of the tool.
- A new edge rinse system was designed and installed on the left dispense module. The new system eliminates the drip problem and has improved process yield.
- Both Suss tools were moved into the new carbon filter room; spare parts were ordered.

Plasmatherm Tools

Installation of the new SiON deposition Plasmatherm tool was completed, as well as vendor tests and final process acceptance and safety-sign-off.

Hot Plate Tools

- A custom hot plate tool was designed and built for 100mm wafers.
- A new style temperature controller for the mask hot plate tool was installed. Temperature is now very stable ($\pm$0.1°C), improving tool process performance and reliability.
- A new hot plate tool with vacuum chuck capability for accurate and ergonomic chuck changes has been received from the vendor.
- A new 'cool-plate' was designed and installed for rapid process throughput of masks.
- A temperature scanning system was designed and built for profiling wafers and chucks which will record temperature characteristics of hot plate systems.
- A second, new hot plate tool has arrived from vendor. This tool has vacuum chuck capability for accurate and ergonomic chuck changes, as well as a mask load/unload feature.
- A new chuck assembly was designed and built for the older hot plate. This upgrade modification will allow use of the new style vacuum chucks utilized on new hot plate tools.

Etch Systems

- Plumbing was upgraded on the KOH etch station to simplify operation and improve reliability. An additional Teflon compact holder was also installed for the second tank, which is an etch station tank.
- New polypropylene compacts are being utilized with no warping after six runs. Product wafers are greatly improved in terms of breakage and reliability. Six Teflon 'thick' compact holders were received from the model shop.

- A compact holder was designed and built for thick and regular compacts for the ethanolamine tank.
- Ultra-Fab Technology has been selected as the vendor for the new fountain cup etch tool. Final design is completed, and the estimated completion date for the tool build is March, 1998 (see section 4.1.6.2).

Sputtered Films Deposition Tool

The new sputtered films deposition tool has been installed and is currently being qualified.

SMIF Pod Activity

- The SMIF Pod clean tool was redesigned and build has been completed. The new design allows universal cleaning of all pods including the new single pod design. The cleaning tool will now automatically sense the type of pod installed and adjust the clean program for the optimum clean cycle.
- The SMIF loader tools were modified to eliminate the tilt feature. Loaders were also modified to handle all formats of SMIF Pods (4-inch, 5-inch, and the new single pod). This new universal modification has saved more than $100K in individual loader purchases.

RTA Oven Tool

- Installation of the temporary tool was completed. The vendor has repaired and calibrated the oven, spare parts have been received, and preliminary safety inspection has been completed. This oven is used for stress relief of the refractory metal process. The new tool is scheduled for delivery 2Q98 (see 6.2.1).

SSI Scorpio Developer Tool

- The SSI tool has been delivered to the MMD; installation and qualification in the MMD is scheduled to be completed by year-end 1997.

New Carbon Filter Room

- Tool Move: Large and small Suss coaters, Yes oven, Blue-M oven, and APT developer tools have been installed in the new carbon filter room.
- New SSI Developer: The tool design layout was completed and work orders are in place. The tool has been installed and is currently being qualified.
- Carbon Room: The new carbon room contains all process tooling associated with the process of chemically-amplified resist. Carbon filters will also contain citric acid for additional chemical removal.

QC Optics Tool

- The chuck was modified with nylon inserts on leveling pads. This will ensure that no minute scratches occur and will improve FM levels.

Bonder Oven Tool

- The thermocouple on the main temperature control electronics was upgraded. Set-up tooling has been adjusted for improved handling and accuracy of bonded parts.

Nomenclature Expose Tool

- The MMD wafer fixture was designed, built and installed on the tool. Initial results appear to be good. The tool will expose alpha/numeric IDs onto wafers, improving defect control; they may eliminate the need for a laser-scribe tool.

Perkin Elmer Photo Tool

- During 1997, the extensive spare parts list was reviewed - there were >$800K in parts in the crib. This was reduced to essentials needed to cover the tool for two years, with risks. The spare parts list was reduced by more than $670K. The excess will be sold to IBM Essonnes. The new replacement tool is expected 3Q98.

Post Apply/Expose Bake Tooling

- A temperature scanning system was designed and built for profiling of wafers and chucks.
- A cold-plate was designed and built for post apply bake cooling.

4.1.3 Miscellaneous Image Placement Experiments

4.1.3.1 University of Wisconsin Modeling Verification

The focus with the University of Wisconsin activity this year has been to provide them with the inputs required to develop and execute models covering the entire refractory process. This includes models on thermal and mechanical distortions during exposure, distortions caused by processing steps, and out-of-plane distortions at each step of substrate fabrication.

The models have been run with the new process, including the current high sensitivity resist systems. Samples of the resists were provided to IBM Yorktown Research to measure the SiC stress and the stress for UVIII and SNR200 resists. The SiC stress measured approximately 100MPa (as expected and quoted by Hoya). The resist stress measured within the sensitivity of the measurement technique, and both resist types showed no measurable change in stress upon exposure. This results in predicted distortions of less than 1nm during exposure.

Thermal models were modified to more correctly simulate the writing technique. With this implemented and with the low exposure doses required for SNR200 and UVIII, the predicted distortions during exposure caused by heating were less than 1nm.

In addition to providing input for the models, we have continued to monitor their results and/or participated in planning for their efforts funded by the Semiconductor Research Corporation, DARPA and Sematech.

4.1.3.2 Small Subfield Evaluation on EL-3+ #6

Small subfield work is resolution-driven and EL-3 #6 was giving 175nm resolution. However, EL-4 P0 will convert to both smaller fields and smaller subfields in 1998 to facilitate 13nm resolution.

4.1.4 FEOL Processing

Refractory stack film levels were tracked beginning on 20 February, and are shown in Figure 12. Defect levels improved throughout the year with the exception of lots 53 and 59. Lot 53 was reworked by removing the films and by redeposition. (Rework was necessary due to a process problem.) It is believed that the rework caused high FM. Lot 59 measured very high FM levels due to surface roughness in the refractory stack, not embedded or surface FM.

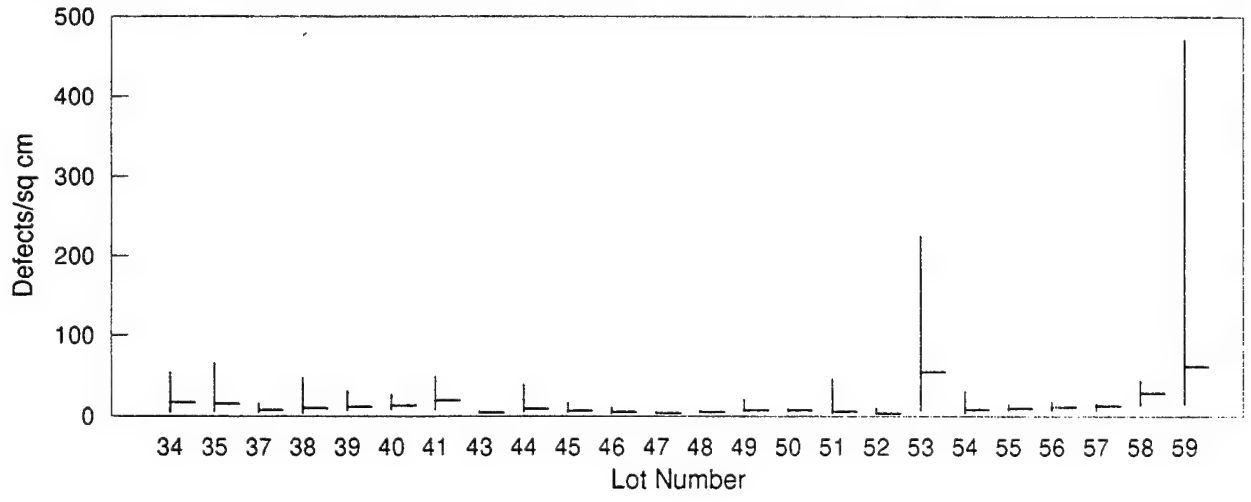


Figure 12. Refractory FM Summary

From 25 November 1997 to the present time, the MMD FEOL has etched 1061 wafers. The films etched into membranes were both silicon carbide and boron-doped wafers. Eight hundred and four membranes were also bonded during the same time period.

4.1.5 Defect Reduction/Inspection

Refractory mask defect levels in the MMD were 70 defects/cm^2 at the beginning of 1997. Figure 13 on page 30 shows the learning since that time. The MMD is currently able to build refractory x-ray masks with defect levels in the 20 to 30 defect/cm^2 range. Figure 14 on page 31 shows the defect classification breakout (pareto chart) for the last five masks inspected. One mask was inspected at 70nm sensitivity and had only 35 defects/cm^2.

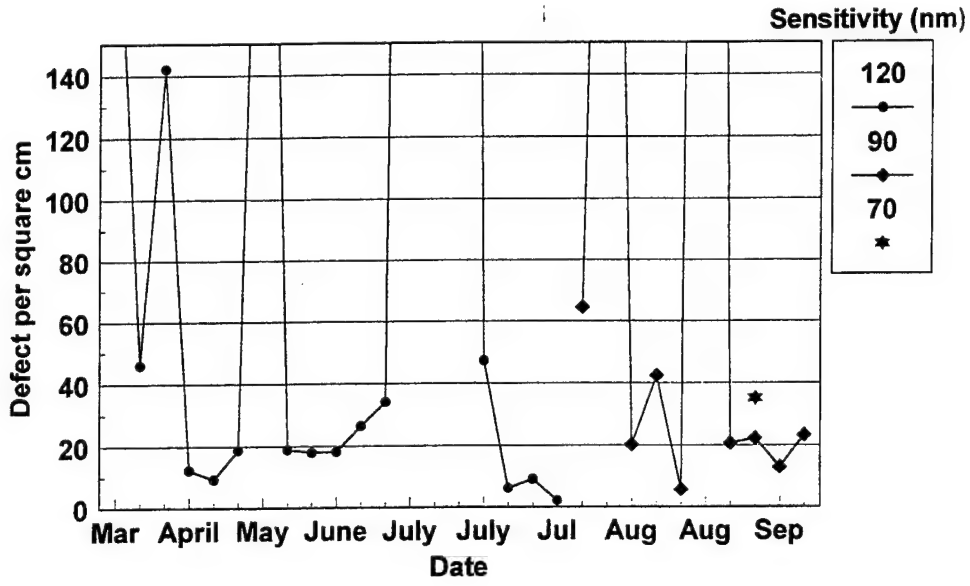


Figure 13. Defects/Current Performance

The MMD began 1997 with approximately 45 non-repairable defects per mask; the current capability is approximately 17 non-repairable defects (see Figure 15 on page 32). Figure 16 on page 32 shows the sources for these non-repairable defects. The majority are attributed to the TaSi deposition. With the implementation of the new SFI TaSi deposition system we expect significant improvements.

4.1.5.1 Inline Tracking of Silicon Carbide Defects

The MMD has been monitoring the quality of the silicon carbide deposition using the KLA SEMSpec to inspect the films. Beginning 7 February 1997, the data shows that, for Tencor, the average defects/cm^2 is 3.47, with a sample size of 34. Those same films averaged 1.83 on the KLA with a sample size of 35. Finally, the final bonded numbers for the FEOL are 4.6 defects/cm^2 with a sample size of 16. The data includes both Tencor tools; most of the KLA data was run at 0.2μm sensitivity.

Code Information

Code	Description	Total	%
11	Opaque Bridge	134	29.8%
12	Opaque Extension	127	28.3%
13	Opaque Spot	60	13.4%
21	Clear Bridge	1	0.2%
22	Clear Extension	27	6.0%
24	Missing Images	9	2.0%
25	Adhesion Defect	4	0.9%
31	Foreign Material	3	0.7%
51	Shifted Images	1	0.2%
71	Opaque Non-Repair	35	7.8%
72	Clear Non-Repair	18	4.0%
73	FM Non-Repair	5	1.1%
81	SiC Blobs	9	2.0%
83	Fish Eyes	6	1.3%
84	Mesa	9	2.0%
88	Clear/Moved Images	1	0.2%

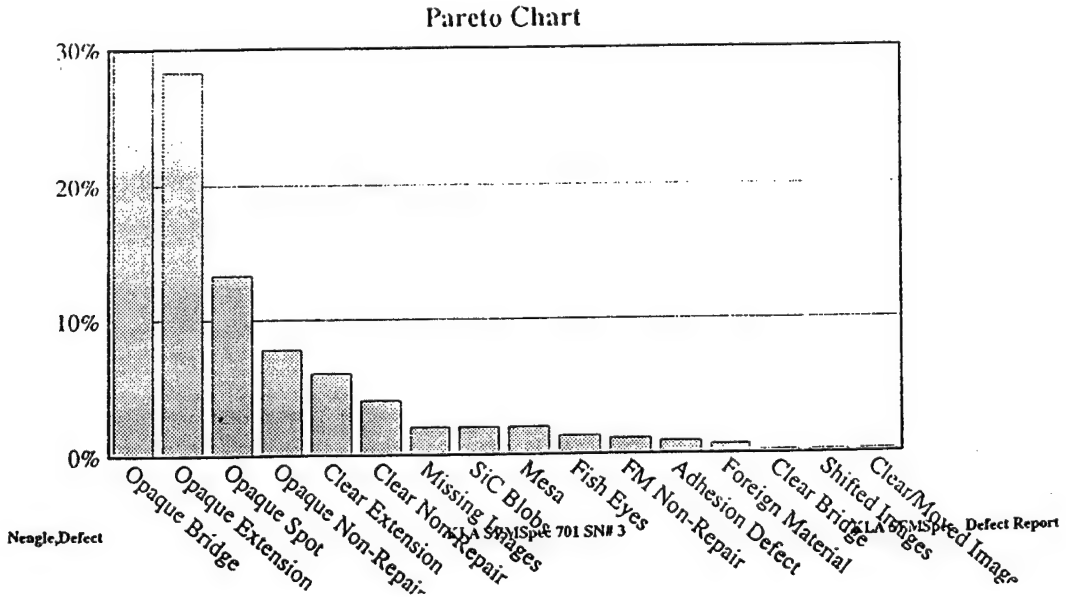


Figure 14. Defect Overview (Pareto Chart)

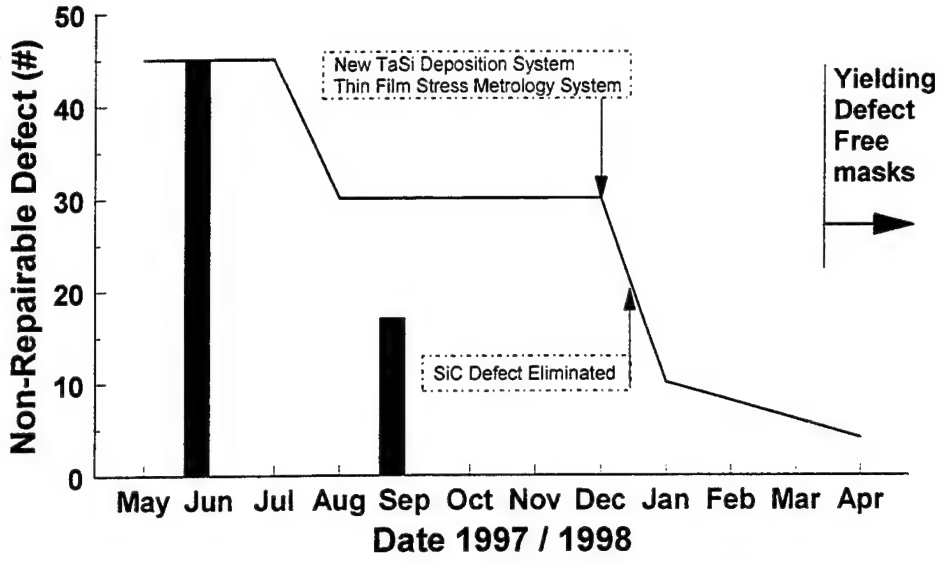


Figure 15. Non-Repairable Defect Learning Goals

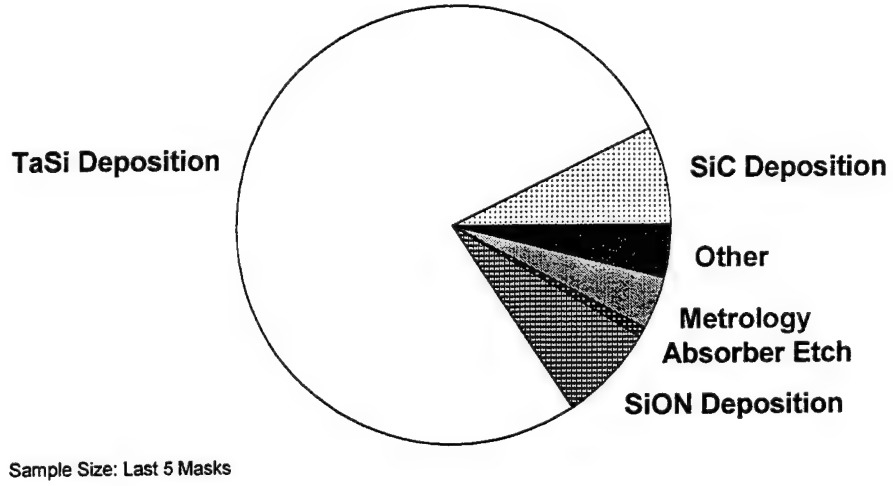


Figure 16. Non-Repairable Defect Sources

4.1.5.2 Absorber (TaSi/SiON) Deposition Defect Reduction

Source acceptance of the SFI Cr/TaSi deposition system was completed. Defect levels of the system were investigated during the acceptance process. The data is summarized in Table 5 on page 33 (note that the system was not in a clean room during the test).

Table 5. Preliminary Defect Results - SEM System		
Film	Defects/cm² 0.250 Sensitivity Average of 10	Defects/cm² 0.550 Sensitivity Average of 5
Cr/TaSi	*3.7*	*0.37*
TaSi	*5.3*	*0.7*
Cr	*0.38*	-
Controls	*0.16*	

For preliminary deposition, the films appeared to be clean. The density of non-repairables causing defects was very low, however.

The acceptance test also included a foreign material adder test. The system, on average, added 0.067 adders/pass/cm².

4.1.5.3 New Mask Boats

The tolerances and dimension of the machined mask boats used by the MMD did not support automation. New Fluoroware boat molds were, therefore, phased into the manufacturing line during 1997.

4.1.5.4 New Mask Boxes

Current boxes used in the MMD line did not properly fit the NIST mask and new mask boxes were phased into the manufacturing line during 1997.

4.1.5.5 KLA SEMSpec Single SMIF Pod Upgrade

The modification to the KLA SEMSpec to accept the single mask SMIF pod was completed during September, 1997.

4.1.5.6 Final Mask Clean

A revised schedule for the mask cleaning project is shown in Figure 17 on page 34. A group comprised of representatives from IBM Yorktown Research, the IBM Strategic Equipment Council and the MMD has been formed to investigate the MMD's cleaning needs and to recommend the best process and equipment-set for each cleaning task. Four tasks are envisioned at this time:

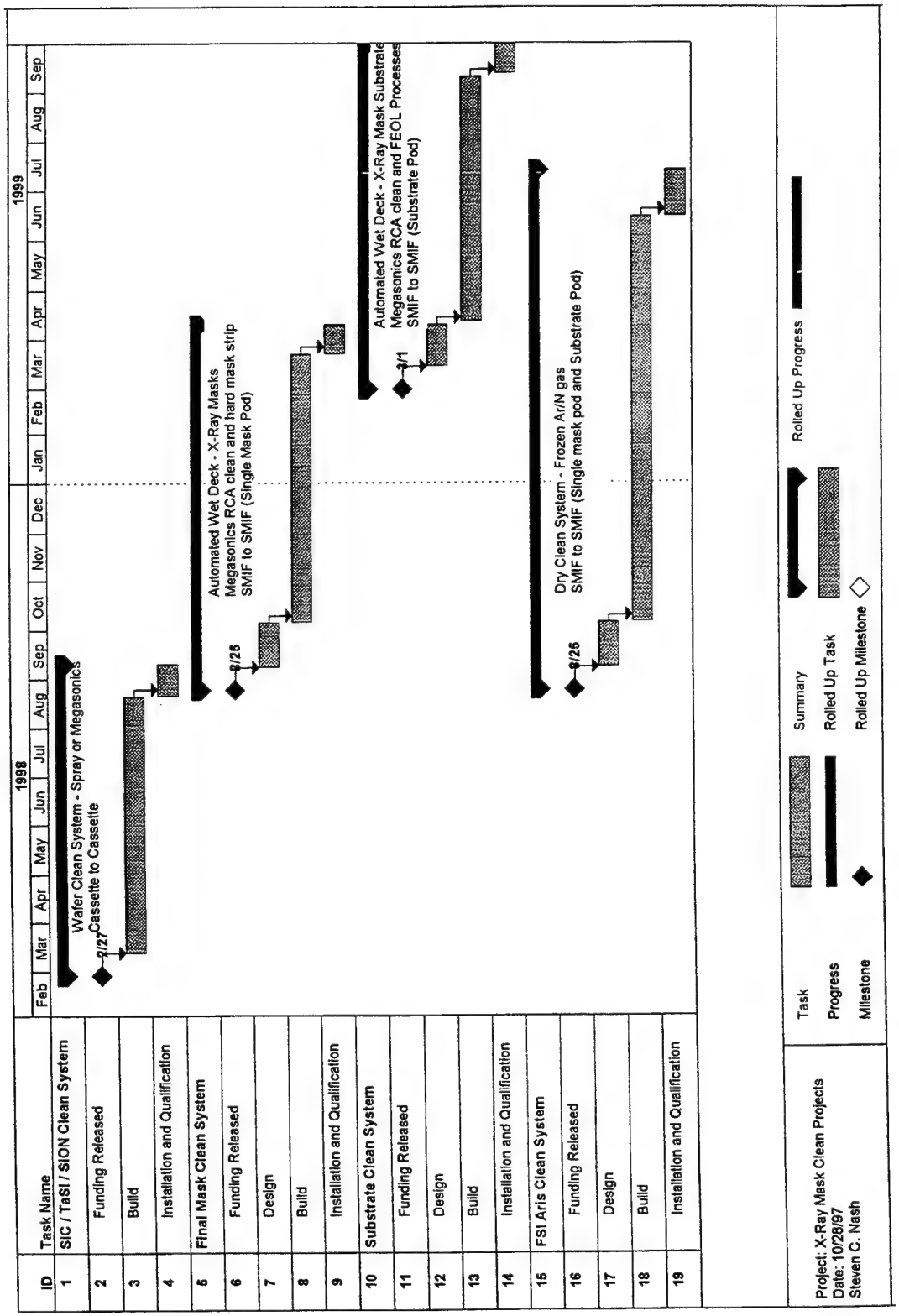


Figure 17. Project Schedule - X-Ray Mask Cleans

1. Wafer cleaning system to support cleaning substrates after SiC, Cr, TaSi, and SiON depositions.
2. Final mask clean system.
3. Replacement to the MMD's megasonics system for substrate cleans.
4. Dry clean system for removing non-repairable foreign material from a completed mask.

All systems should be fully automated, with integrated SMIF and class 1 mini-environments.

4.1.5.7 Back-Side Lithography System

A replacement is needed for the MMD's Perkin Elmer 500 which is used for back-side lithography. The Perkin Elmer 500 leaves chuck marks on the front surface of the x-ray masks, as shown in Figure 18 on page 36. A statement-of-work was developed and submitted to several optical aligner companies for review. Quotations were received from Karl Suss and Electronic Visions and are currently being reviewed. Capital funding for this project is being pursued. The overall project plan is shown in Figure 9 on page 15.

4.1.6 Substrate Flatness/SiC 2.1mm Wafers

As the focus continues to shift toward 100nm and below, wafer flatness becomes a very important issue. Additional focus will be placed on this during 1998. The substrate data has been plotted and analyzed to serve as a benchmark of the current performance. The University of Wisconsin has modeled some of the improvement strategies including thick wafers or alternate rings. MMD and ALF met on 11 November 1997 to discuss long-range plans and requirements.

4.1.6.1 2.1mm Thick Wafers/5μm Flat Substrates

All tooling modifications to build 2.1mm prototypes have been completed with the exception of Flatmaster. Twenty SiC depositions on the thick wafers are ready for processing. The project plan has been updated (see Figure 19 on page 37).

A prototype bonding fixture has been designed and is being built (see Figure 20 on page 38).

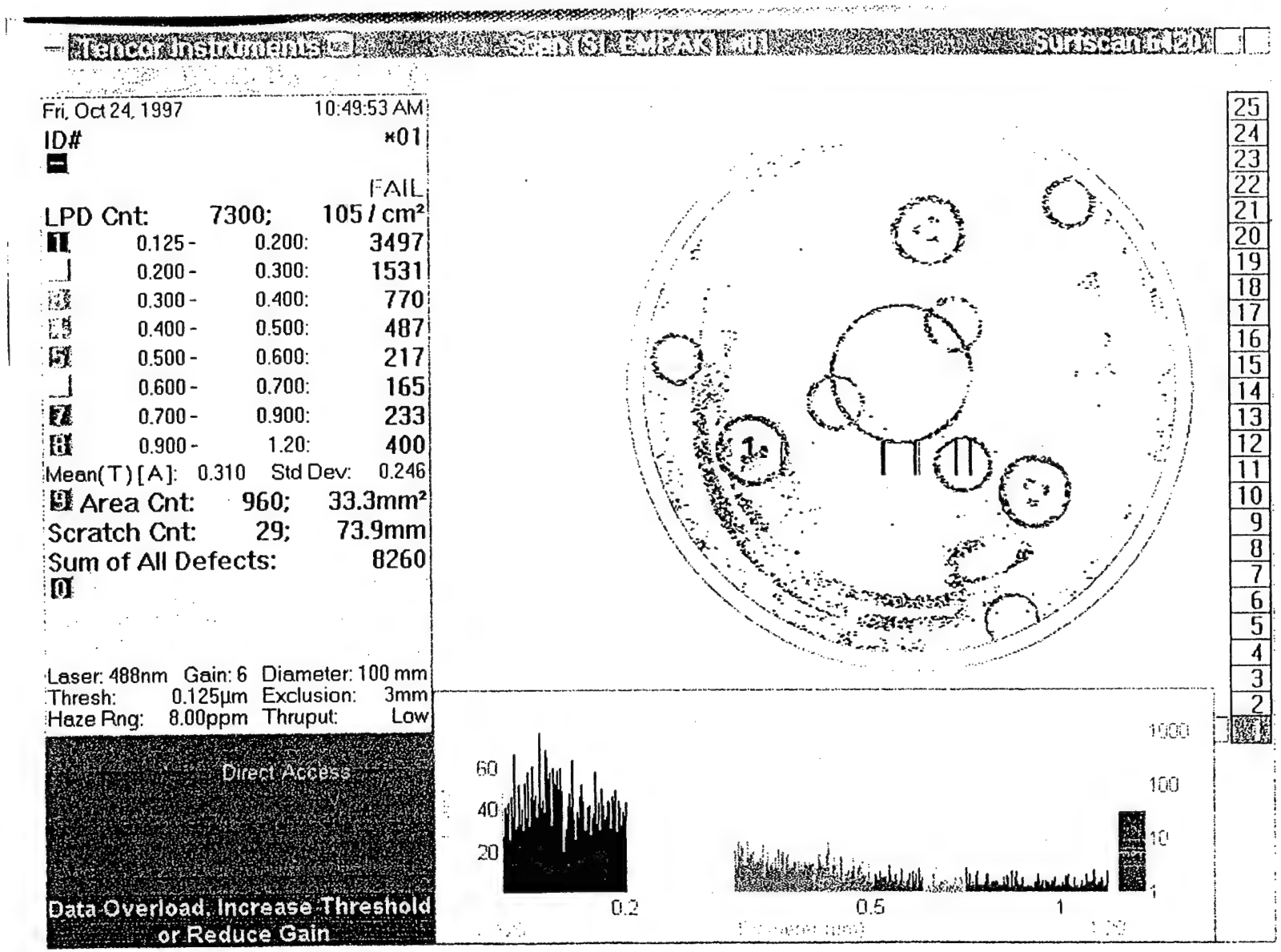


Figure 18. Backside Lithography

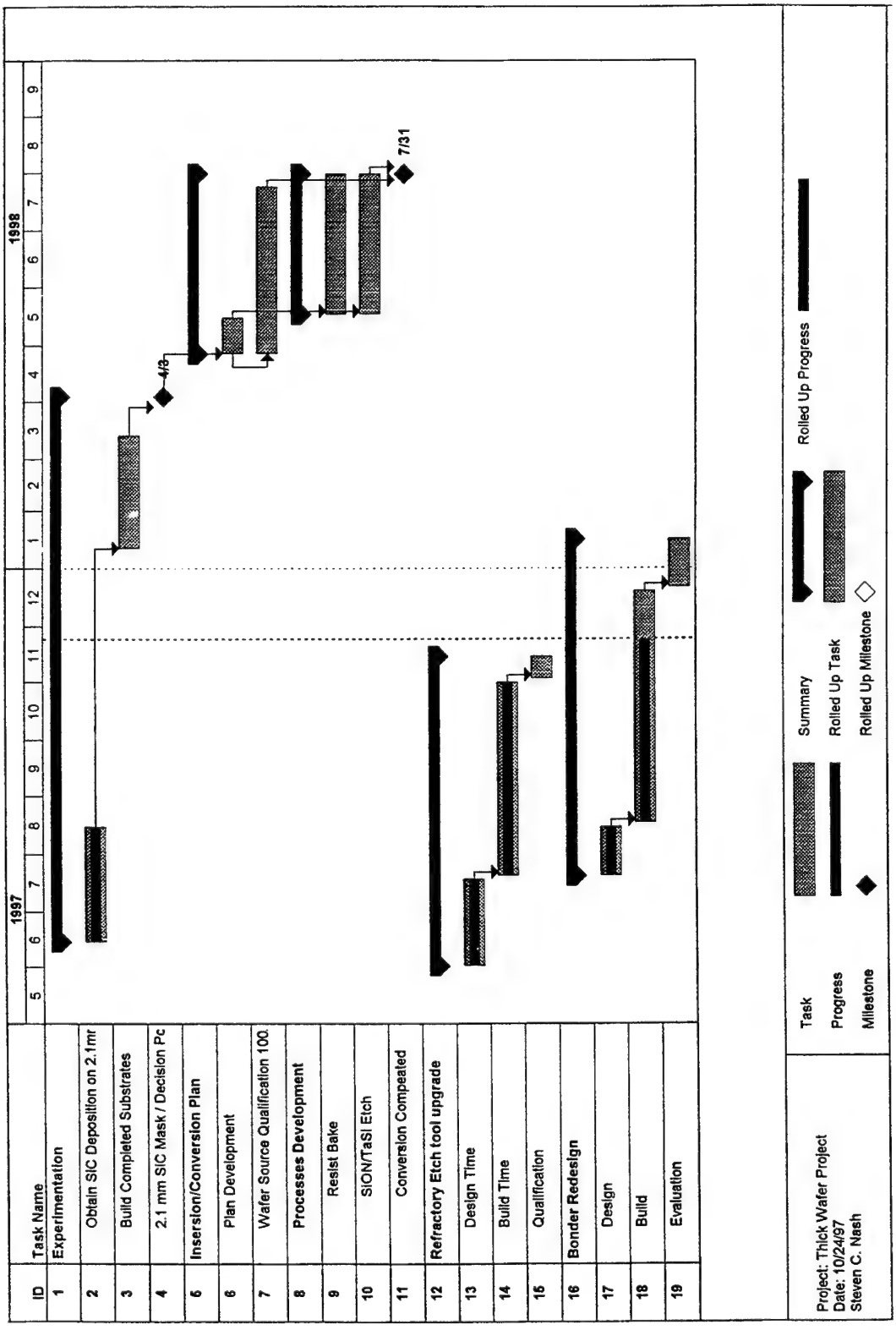


Figure 19. Thick Wafer Project

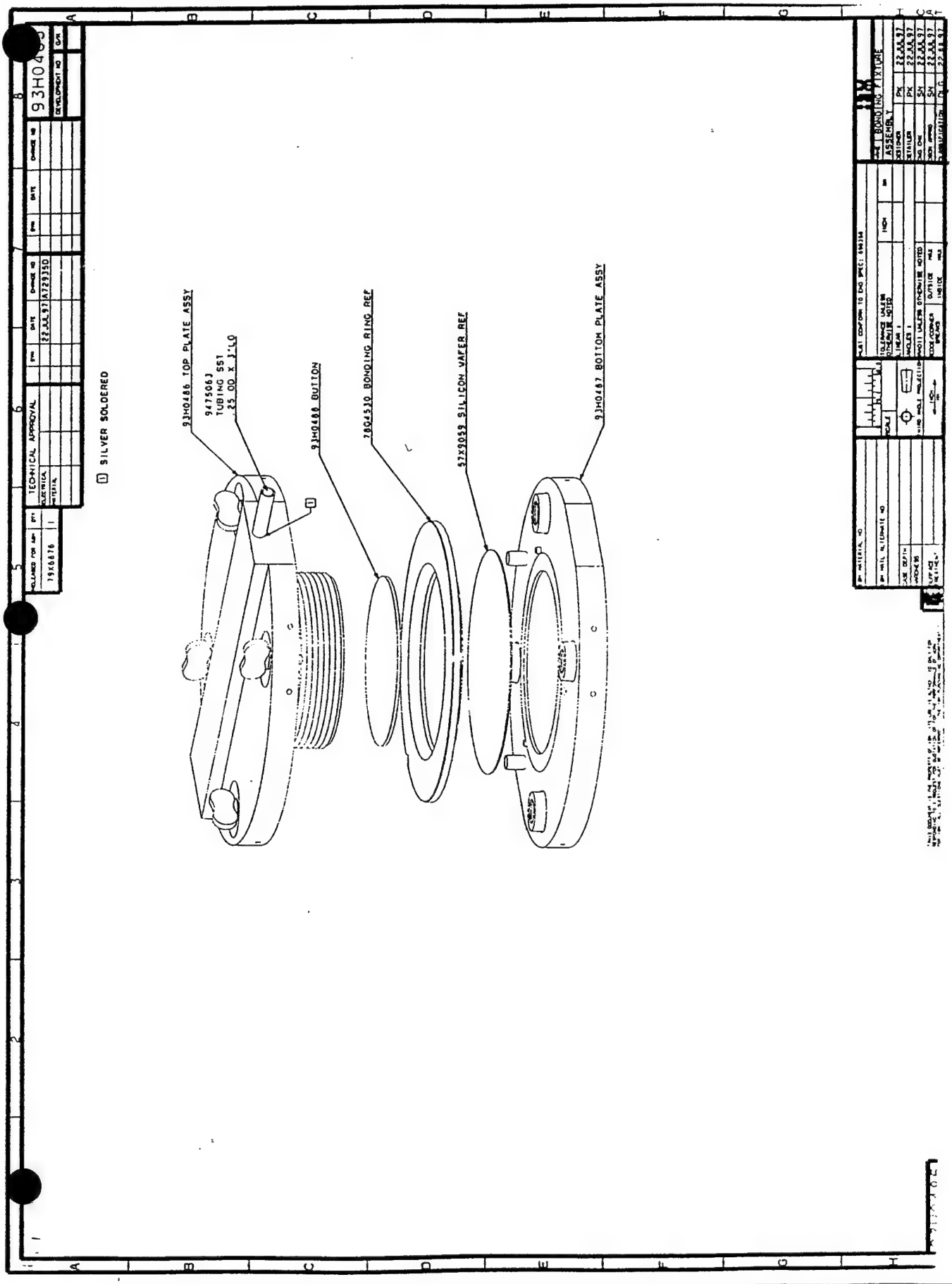


Figure 20. Prototype Bonding Fixture

4.1.6.2 Etch Chemistry/Tooling (Fountain Etch Station)

KOH was selected as the etchant for SiC membrane masks and an interim process was implemented on the line. The long term plan is to use a fountain etch approach. Capital funding for this project was released in June, 1997 and the fountain etch station (Figure 21 on page 40) was ordered from Ultra Fab. The shell design review has been completed (see Figure 22 on page 41 and Figure 23 on page 42).

4.2 Develop 0.25μm Production Mask Fabrication Capability (Task 3.3)

Task Objective: ***Establish and maintain a pilot production facility capable of on-premises x-ray mask production, and demonstrate 0.25μm mask fabrication capability by fabricating production masks.***

4.2.1 PMMA Resist Status for EL-4 P0

The PMMA process was phased out in late April after the Phoenix AA and GC, the last gold product masks, were successfully manufactured and shipped. The PMMA process was replaced with UVIII positive resist, which is dry etch resistant (required for refractory metal masks). The line monitors were also converted from gold absorber masks to refractory masks with the new resists (both UVIII positive resist (Falcon) and SNR negative resist (Nighteagle).

4.2.2 SNR 200 Resist Status

Resist scumming was observed on several refractory masks with the SiON hardmask. The original process design of experiments (DOE) matrix was completed for the Cr hardmask.

A second DOE was completed to determine the optimum SNR process on the SiON hardmask. The variables were post-apply bake (PAB) temperature, post-expose bake (PEB) temperature, and developer normality. The figures of merit included exposure latitude, dose-to-print and, most importantly, scumming.

DOE analysis indicated that the optimum process is a PAB of 120°C, PEB of 110°C, with a developer concentration of 0.14N TMAH. The exposure latitude was approximately 18%, the dose-to-print was 18μC, and the scumming score was four out of a possible score of five.

The process was implemented on 16 June 1997 based upon the DOE results, and product was monitored for scumming. NIGHTEAGLE image size data indicated an upward shift in image size x-bar with the new process. A dose adjustment was made on 20 August 1997 from 22μC to 19μC, resulting in an x-bar improvement.

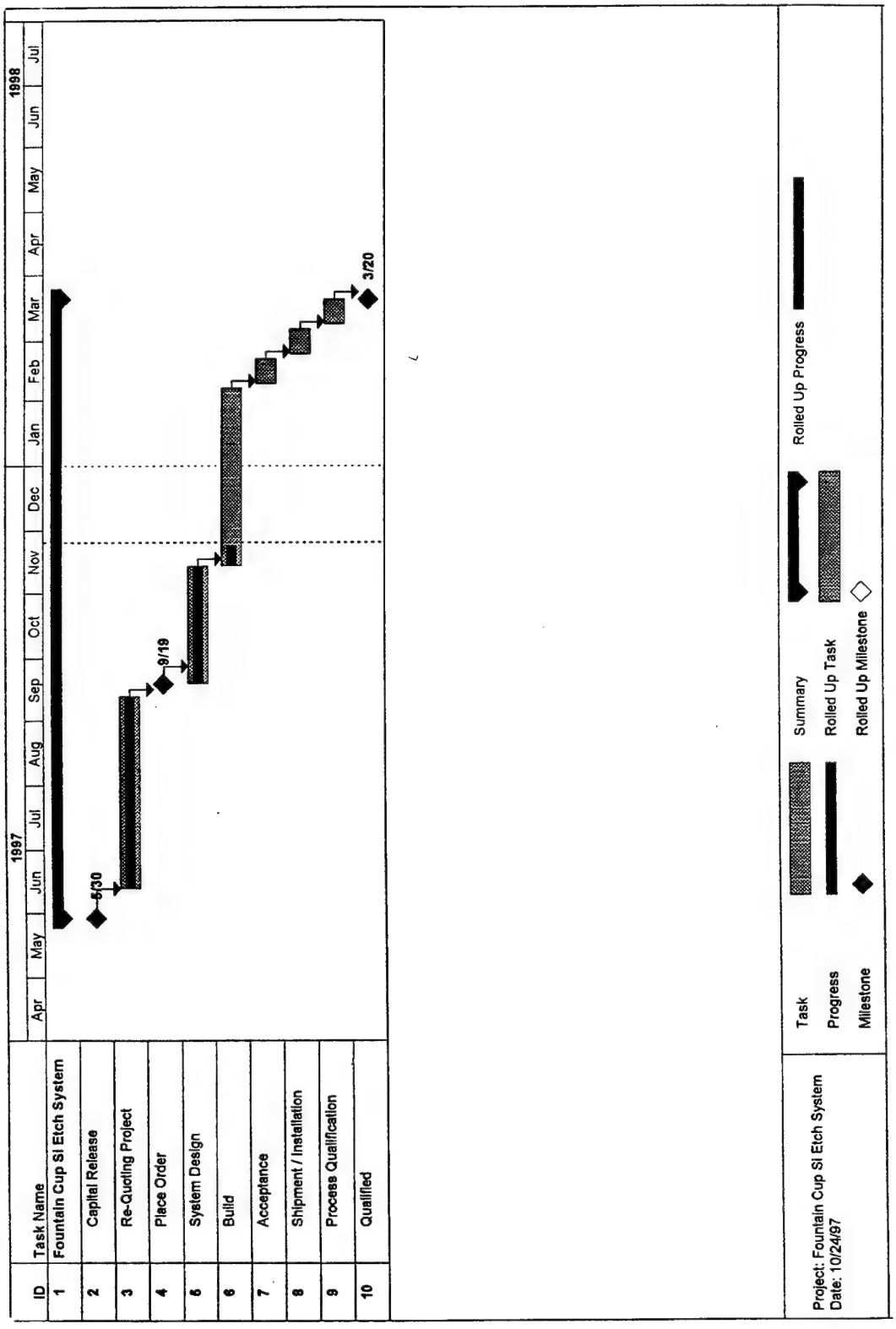


Figure 21. Fountain Etch System

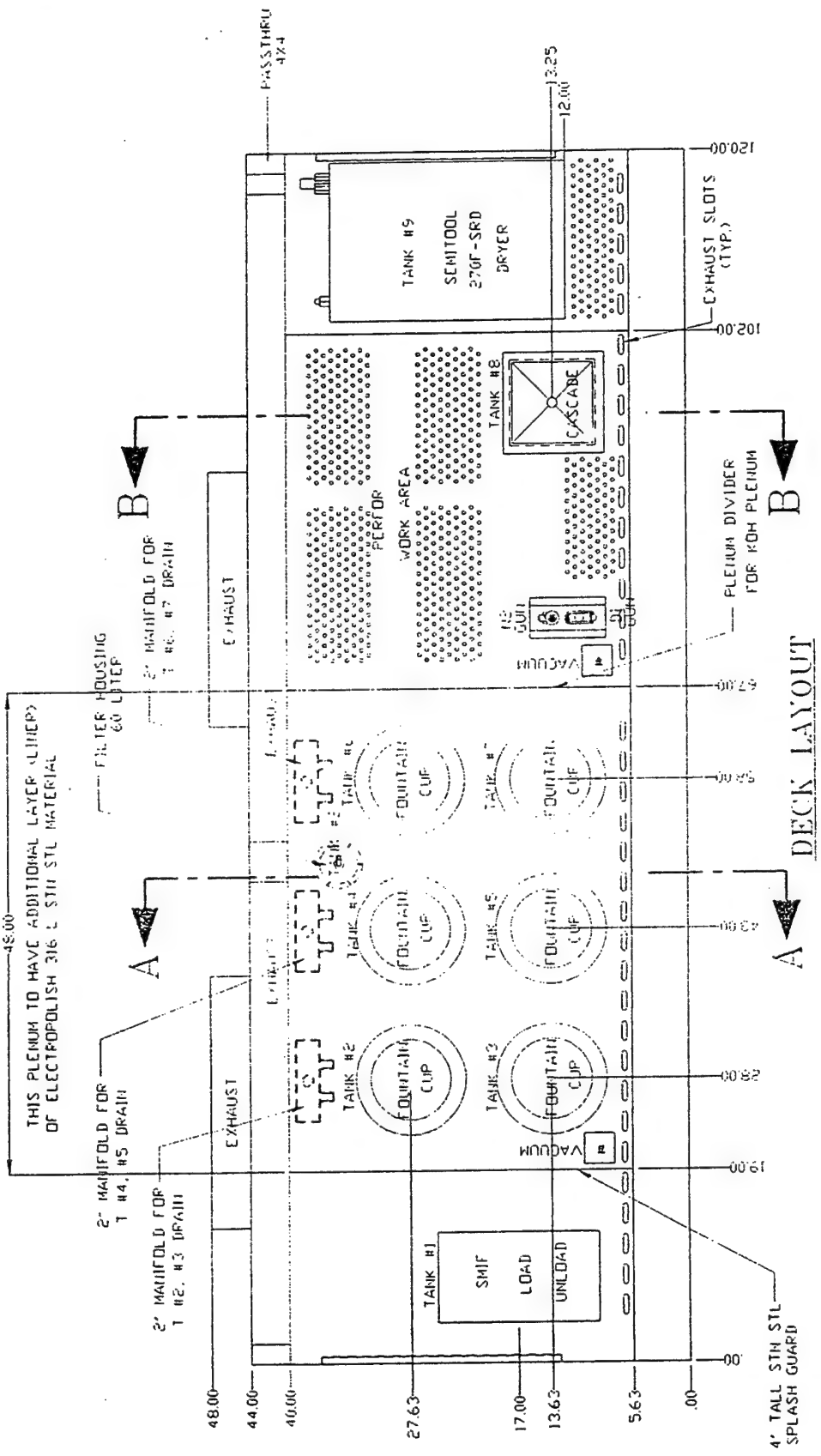


Figure 22. Shell Design - Fountain Etch Station

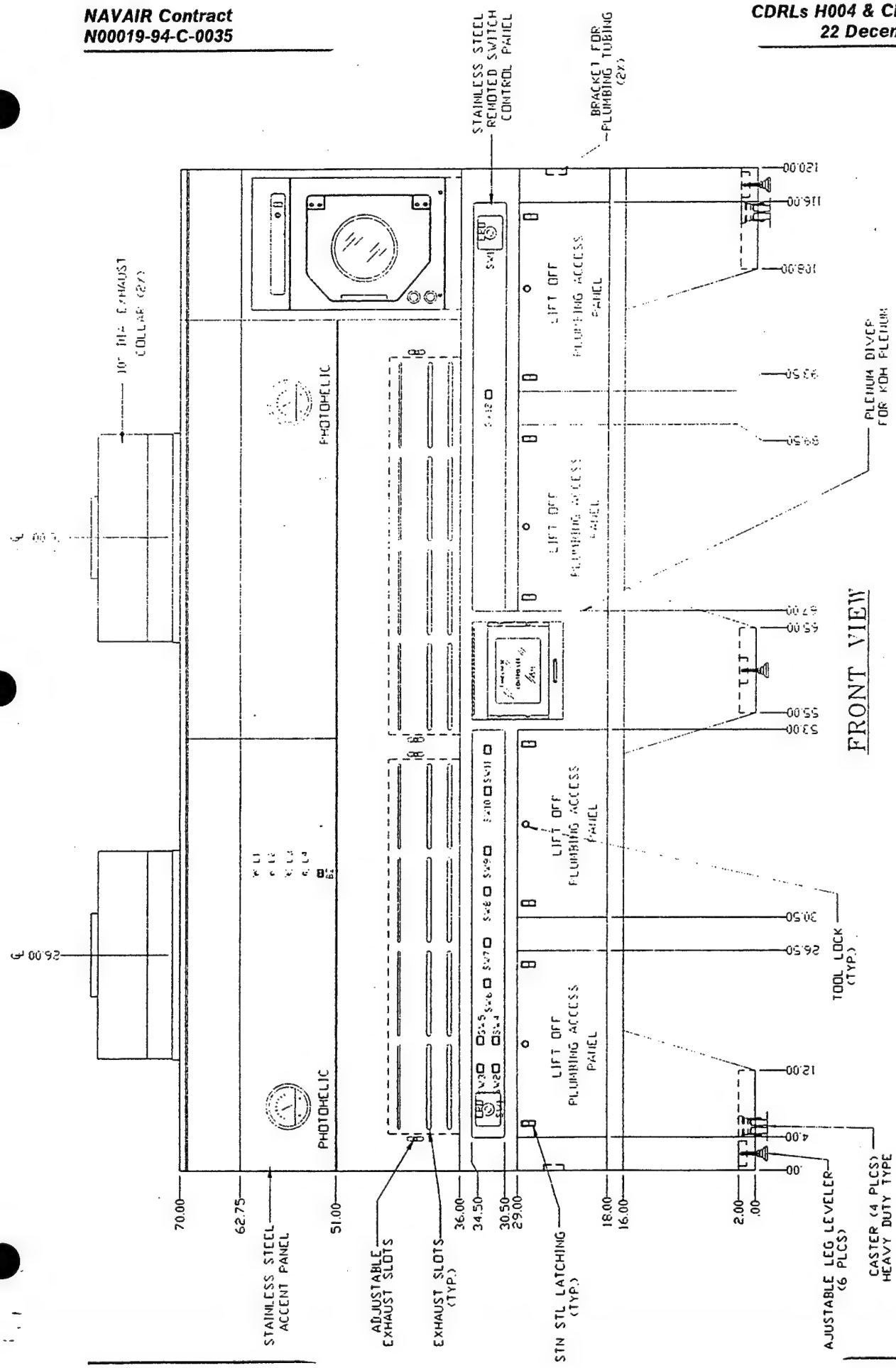


Figure 23. Shell Design - Fountain Etch Station

A resist de-wet problem was observed on some membranes during SNR resist application. An HMDS flask leak was found and repaired, and fresh HMDS was installed, significantly reducing the problem. Occasionally, small de-wets are seen on a small number of substrates which are possibly caused by substrate contamination.

The dose for SNR 200 resist on EL-3+ #6 (15μC/cm^2) has been verified using the NIGHTEAGLE pattern, and EL-3+ #6 has proven to be a viable backup for EL-4 P0. In October, the decision was made to convert EL-3+ #6 to a chrome-on-glass writer.

4.2.3 UVIII Resist Status

UVIII is a positive, chemically-amplified resist which was evaluated in 4Q96 as a positive resist complement to SNR 200 negative resist. The UVIII DOE was completed in 1Q97 to optimize the bake conditions for this new resist. Thirteen trials were completed at temperatures for PAB and PEB ranging from 135°C to 145°C. The figures-of-merit included exposure latitude, resolution and dose-to-print. The EXPERDESIGN, an IBM internal software program, analysis indicted the optimum PAB temperature of 137°C with a PEB at 143°C. Excellent exposure latitude and image resolution of 75nm were achieved. The exposure dose of 18μC/cm^2 was chosen for UVIII on P0 and verified using the benchmark pattern.

The UVIII process was implemented for EL-4 P0 test wafer focus series on 20 August. A bonded wafer process has also been established for emulated L-patterns for pattern placement.

A delay study was completed using the daily test wafer to determine the shelf-life of coated wafers. The results indicated that the wafers are acceptable for at least 14 days.

Several product patterns have been written to complete the qualification of UVIII resist, including the IBM 1Gb test site with 175nm critical features, IBM 165nm logic test site, IBM 250nm logic test site with an embedded SRAM, and the 175nm Falcon line monitor (reverse tone NIGHTEAGLE). Three lots of UVIII resist were compared for both chemical analysis and functionality, with favorable results. Therefore, the resist qualification was successfully completed and the results were documented in a Technology Assessment Report in October (CDRL G004, 97-MMD-LMFS-00076).

4.2.4 Thin Resist

The initial thin resist experiment was completed using SNR resist. The results showed less scumming with 3000Å resist as compared to 4000Å. For example, for the thin resist 100nm lines by 200nm spaces were free of scum, while for the thicker resist 100nm lines by 250nm spaces were free of residue.

The next thin resist experiment will be completed using thin UVIII resist since SNR will be replaced with UVN2 in 1998.

4.2.5 Image Size Characterization

Image size 3σs for August and September ranged from 17 to 33nm on the NIGHTEAGLE masks. Image size plots showed a left character; that is, smaller images on the left edge of the mask, for both P0 and EL-3+ #6 parts.

Several experiments were completed in an effort to determine if the hotplate (HP) was the cause of this image size character. The original hotplate without shuttle was compared to the newest hotplate with the shuttle:

X072397B new HP x, 3s = 199, 15nm left character
X072397C orig. HP x, 3s = 198, 17nm random character
X072297G new HP x, 3s = 202, 23nm missing meas., no plot
X072297H orig. HP x, 3s = 147, 14nm no plot

The PEB was completed on the original hotplate for all product as of 11 September 1997, since this limited data indicated this might improve the 3σs.

The alignment of membranes on hotplate was checked for all pedestal types using setup (broken) membranes, as shown in Table 6.

Table 6. Hotplate Alignment

	New Hotplate	Original Hotplate
NIGHTEAGLE	*Left and top largest gap*	*Top and right largest gap; not as large as for hew hotplate*
Phoenix	*Top and slightly left, not as bad as other pedestals*	*Top and slight gap, not as bad as other pedestals*
F45P	*Top and left, not as bad as other pedestals*	*Top and right, not as bad as other pedestals*
50x50	*Left and top largest gap*	*Top and right largest gap; not as large as for new hotplate*
Viper	*Top, left and right gap*	*Top and right worst gap*

The new hotplate was not centered as well as the original hotplate and the Phoenix and F54P had smaller gaps than the other pedestals. The new hotplate was recentered for all bake chucks on 29 August 1997.

Each pedestal size was measured and compared with membrane size and with prints given to the model shop. The model shop accuracy was found to be very good (within 0.03mm of print). A gap size variation for the different pedestals was observed:

Nighteagle 0.99 × 1.0mm
Mach V 0.91 × 0.93mm
Viper 0.89 × 0.9mm
50x50 0.91 × 0.91mm
F54P 0.71 × 0.67mm
Phoenix 0.32 ×X 0.29mm

The F54P and Phoenix pedestals were ordered with a 0.7mm gap. Based upon problems experienced with Phoenix parts "seating" on the chucks, the gap was increased to 0.9mm for all other pedestals. The actual cause of the problem was an error in the bake chuck print - the gap was only 0.3mm. Based on the above, a bake pedestal with a 0.5mm gap and no vent was ordered. (The vent is on the left corner where image size is smallest.)

An experiment was completed to evaluate the new 0.5mm NIGHTEAGLE pedestal and the results follow:

New Pedestal: no vent 0.5mm gap:

27A5 X092997D x, 3s =	184, 14	Left char. still observed
49B4 X100697C	182, 13	Left char. still observed
36B5 X100697D	198, 12	Left and bottom small
36B1 X100997B	184, 11	Very slight left char.
36A5 X100997C	184, 15	Slight bow
AVERAGE 3σ	13nm	

Controls with old pedestal: with vent groove and 1.0mm gap:

36A1 X100697B x, 3s =	198, 15	Slight bow
25C4 X100997D	182, 17	Bottom small
AVERAGE 3σ	16nm	

A small improvement in average 3σ (within measurement noise) was observed with the new pedestal, yet character difference was not seen. Some other change occurred during this experiment since the part-to-part variation (11 to 17nm) is significantly smaller than for product run in August and September (17 to 33nm).

The results to date with the new 0.5mm pedestal have not proven that this pedestal is better than the old pedestal with the 1.0mm gap. The high 3σs (in the 30s) seen on product baked on the old pedestal prior to this experiment are probably not caused by seating on the hotplate because with a 1.0mm gap there is ample tolerance for bonding centrality and operator positioning. Additional data will be obtained to determine if any improvement can be realized with the new pedestal.

The hotplate was profiled with the pedestal using a Fluoroptic thermometer: 1.0°C variation (range) was observed. This variation (if the measurement is accurate) would result in an image size variation of about 10nm for SNR and 5nm for UVIII resist. This means that the 3σs for UVIII should be half (or significantly better than) those of SNR if bake is the primary source of the 3σ error. (Falcon data will be obtained to determine if this is true.) The hot plates will also be profiled with IBM Yorktown's infrared camera as soon as the camera is available.

A mask with the left character was remeasured with 3× measurement sites and with images closer to the right edge. A bow character was observed indicating the "left character" was a function of the measurement package.

In addition, four masks have been processed with an oven bake to evaluate the image size character using this process. The bake temperature was too high and a lower temperature will be tested.

A helium bake experiment was completed using the full Viper array. This experiment was inconclusive due to poor image quality. This experiment will be rerun using helium-cooled Plasmatherm at 80°C once oven the bake process is defined.

Fogging experiments are also being designed to determine the contribution of this factor to the image size errors.

4.2.6 Status of EL-4 P0

The EL-4 P0 system has continued to satisfy user requests throughout the contract period. Unplanned tool down time for 3Q97 was held to less than 10% during the second quarter, and for fourth quarter, 1997 to date, unplanned down time is at 15%. The emphasis at EL-4 PO continues to be the delivery of needed MMD masks to the required specification. Time was scheduled during this quarter for weekly tool assessments and for implementation of experiments and solutions. Work has continued on the noise issues that were identified previously and reported in the quarterly progress reports (CDRL H004). Efforts have centered on two areas of beam control: 1) alignment drivers in the Column Control System, and 2) noise in the Major Magnetics. It was found that the drivers for the sixth alignment coils were generating noise at the digital-to-analog converters (DAC). The full range of this driver was ±100ma. This was reduced to ±25ma to reduce the least significant bit (LSB) weight at the DAC. Steps have also been taken to reduce the noise level in the Major Magnetic drivers. Several iterations of adjustments have been done to decrease the noise level and the settle time. The work has yielded an improvement in the placement at the tool when measured with the reference plate (REFP) diagnostic. One-sigma numbers were previously in the 8-9nm range and, after the current work, have dropped to the 3-4nm range. The target for this work is a 1-2nm range. The Eddy Current compensation network that had previously been dormant, was recently activated to reduce the within-field forward, backward error. This was necessary due to the faster, low dose resists that are in use. There has been an increase in failures because of mechanical wear-and-tear at the tool. Several components have exceeded the recommend lifetime, most notably the four model 95 PCs that are used to operate the tool LAN (local area network), tool controller, and the user interfaces. A plan has been put in place to upgrade these machines to Pentium-based systems with faster clock speeds and larger drives for program storage. These systems will be phased in over the next few months with little or no impact. A schedule has also been put in place to upgrade the tool to improve the placement performance. These upgrades are grouped into three categories: 1) smaller subfield/fields with 1 bit positional DACs, 2)

laser upgrade to a Lambda/1024 system, and 3) replacement of the Major Magnetics with a redesigned EL-5 type of system. These will all mimic EL-5 type systems which will allow better serviceability across the two platforms. These three upgrades will be integrated into P0 over the next year, with the change to smaller fields and subfield coming by the end of 4Q97.

4.2.7 Status of EL-3+ #6

EL-3+ #6 had limited use in 1997. Several NIGHTHAWK masks that were exposed on this system were shipped during the first half of the year. Initial results from both NIGHTEAGLE and VIPER line monitors were promising, and one level of the IBM 1 Gbit test pattern was fabricated during the third quarter. Image placement limitations and substrate availability necessitated only test exposures on EL-3+ #6 in the fourth quarter. An assessment underway to determine whether to take this tool offline.

5.0 Advanced Lithography Defect Verification

Several major advances were made in ALF during the Option 2 contract period. A new scanning mirror gave better exposure uniformity at higher flux. Four levels of a 1Gb integrated lot test site were exposed with x-ray and electrical testing indicated functional devices. ALF implemented 24 hour per day unattended operation of the ESR, as well as weekend runs. Finally, ALF moved to prepilot operations with the exposure of 3000 wafers during a 12 day, 24 hour per day lifetime study with minimum downtime.

5.1 Tooling

5.1.1 Suss Stepper

During this contract period the second Suss stepper was retired from operation.

5.1.2 Overlay Tools

Early in this contract period, the Conquest overlay tool was replaced with a prototype Biorad Q2 tool. The Biorad tool proved to be too unreliable for routine use and it was replaced with the KLA 5015. The KLA was subsequently moved into the clean room and is the standard ALF overlay tool. It has also been modified for more automatic cassette-to-cassette operation.

5.1.3 ALF Beamlines and Mirror

As reported under Option 1, the segmented scanning beamline mirror did not meet specifications at two of the three mirror joints. In March, 1997 it was replaced with a single segment mirror. The new mirror is heavier and required some modifications to the mounting hardware in the mirror box on the beamline. The installation was successful and the scan perturbations from the segment joints are gone. The exposure uniformity was then measured as $\pm 1.3\%$ over the full 50×50mm field, as shown in Figure 24 on page 49. Table 7 on page 50 shows that the variation in ACLV from exposure is now in the statistical noise level.

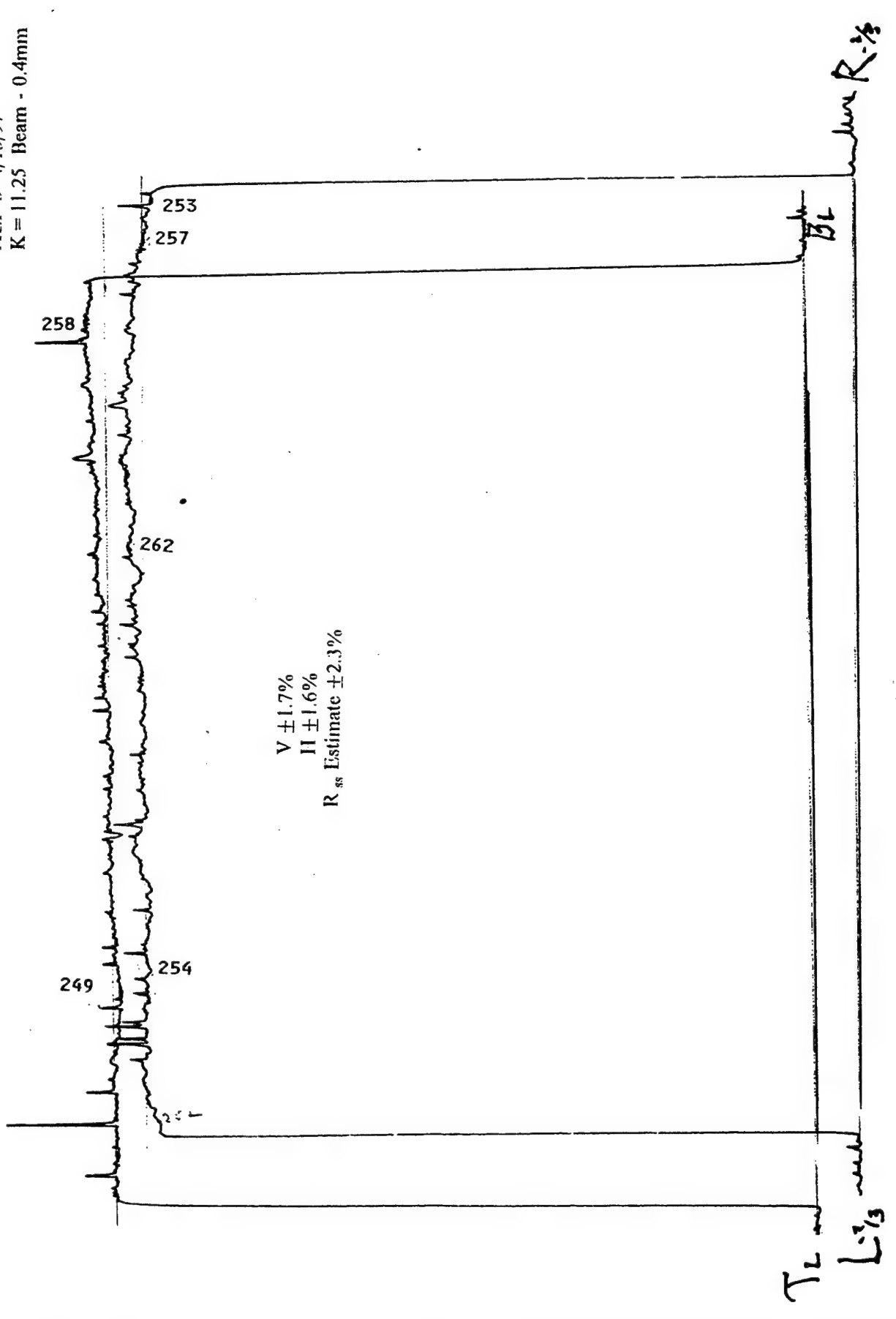


Figure 24. Single Scan Estimate - ALF-3 Uniformity (Recorder Plot)

Table 7. ACLV Means and Standard Deviations			
	Mean (nm)	St. Dev. (σ) nm	Added to mask, nm(RSS)
Mask	*-170*	*18*	
Wafer #1	*163*	*19*	*6.1*
Wafer #2	*165*	*18.4*	*3.8*
Wafer #3	*164*	*19.1*	*6.4*
Wafer #4	*164*	*18.5*	*4.3*

Several software improvements were also made to the ALF 3 beamline. The first improvement was to switch from TCP to UDP communications protocol, shortening communications time from several hundred milliseconds to the 30 to 50 millisecond range. The second was to allow the scan mechanism to use the full travel available to optimize the scan acceleration, therefore reducing the deceleration dwell time to 0.5 seconds which is the same as the stepper overhead. This has resulted in a noticeable improvement in wafer throughput.

5.1.3.1 Other Beamline Activities

The ALF 1 beamline has been modified to use as a radiation-damage beamline. The line was vented and a new focusing mirror has been installed along with a new window. These have been conditioned and aligned. A flux increase of about a factor of 8 is now available for small area radiation damage studies. The exposure field is approximately 6.5×14.5mm. The 6.5mm width maximizes the distortion produced by radiation damage for mask membrane sizes of about 20×20mm, making this a rapid indicator test for mask materials. Radiation damage studies have been started on masks.

5.1.4 ESR Repair, Upgrades and Other Activities

The source was modified in 1996 during Option 1 to allow for larger beam currents. Subsequent beam studies showed that the modifications were successful. Substantial beam steering was now possible in both dipole magnets. Beam heating of the cryogenic system was substantially reduced from the levels prior to the upgrade and consistent with normal operations. Initial beam lifetimes were short. A program of around-the-clock stored beam conditioning achieved acceptable beam currents and lifetimes by late in the last period. Several more changes were made to the system which permitted unattended overnight running of the synchrotron. This has been the normal mode of operation for this period.

One day per week has been devoted to source studies (and maintenance). Much of this time has been spent on studies to increase the peak current and then to increase the lifetime of the large currents. A highly efficient repeatable ramp for high peak currents has been developed, but presently the peak current is limited to 320mA due

to beamline window constraints. The light source has experienced greater usage during this contract period. Operation is now tracked from 6:00am Monday to 6:00pm Friday. This increased usage came with no increased manpower requirements due to the implementation of fully automatic overnight running. The increased usage did not affect downtime until a klystron failure in August, 1997.

The source team has continued to work on storing larger beam currents. Currents over 600mA have been stored on several occasions, with a maximum beam of 640mA and an indicated lifetime of 10 hours. Whenever possible, beams of about 500mA are stored in the ESR to beam-clean the system. The 500 MHz prebuncher failed on the linac during this period, but the source team was able to continue normal injections, although slower, until it was repaired.

A special control sequence has been written and tested which will put the system into standby mode in the event of a problem. This has permitted the ESR to be operated over the weekend in unattended mode. ALF is now running the ESR 24 hours per day for 7 days a week with operators in attendance only during the usual ALF extended single shift hours. The annual maintenance shutdown was held the last week in July. Late delivery of some parts delayed the start up for a few hours.

The klystron on modulator 1 failed on 20 August. (This klystron is necessary to run the linac and inject electrons into the ring.) The spare klystron also failed after only one hour of operation. In both cases one of two filaments failed. Modulator 2 (unused) was turned on and for about two weeks, injection was successful with both modulators running at partial output power. The klystron in modulator two then started to arc internally which prevented its use. Oxford Instruments involved the Klystron manufacturer and also brought in consultants from England to address the problem. A low energy injection procedure has been commissioned which allows the ESR to be filled with the spare klystron at partial output acting alone. Also, the klystron in the second modulator is being conditioned to ever-increasing voltages with the possibility that it can be brought back to operating condition. Injections are somewhat slower and not as robust as before, but a blackheat mode of klystron operation has been established and the 74MeV mode of injection is now generally robust.

Plans are in place to have one of the failed klystrons rebuilt at the factory. This is the first significant electrical failure in the system in five and one-half years of regular scheduled operation and two prior years of test and commissioning. It is felt that the stress of the 24 hour/seven day operations may have contributed to the failure. Table 8 on page 52 plots the uptime (as measured by the Sematech E-10 standard) of the light source.

Figure 25 on page 53 shows the dramatic increase in usage of the light source during the last two years.

Table 8. Long Term Availability

Quarter End Date	Scheduled Hours	UPTIME			DOWNTIME				Major Upgrade	% Availability Helios
		Productive Hours	Engineering Time		Sched Down		Unsched Down			
			Hours	%	Hours	%	Hours	%		
31-Mar-92	547	466	16	2.9	0	0.0	65	11.9	0	88.1
30-Jun-92	477	415	44	9.3	0	0.0	18	3.7	0	96.3
30-Sep-92	529	477	20	3.8	0	0.0	32	6.0	0	94.0
31-Dec-92	564	547	16	2.8	0	0.0	1	0.1	0	99.9
31-Mar-93	440	415	22	4.9	0	0.0	3	0.8	0	99.2
30-Jun-93	536	352	137	25.5	45	8.4	1	0.3	0	99.7
30-Sep-93	540	366	58	10.8	113	20.9	3	0.7	0	99.3
31-Dec-93	510	424	36	7.1	48	9.4	3	0.6	0	99.4
31-Mar-94	518	405	0	0.0	104	20.1	9	2.1	0	97.9
30-Jun-94	570	455	14	2.4	100	17.6	1	0.1	0	99.9
30-Sep-94	586	527	5	0.9	40	6.8	15	2.8	96	97.2
31-Dec-94	598	483	22	3.7	92	15.4	0	0.1	0	99.9
31-Mar-95	579	443	54	9.4	72	12.4	10	1.9	0	98.1
30-Jun-95	570	488	33	5.7	48	8.4	2	0.4	0	99.6
30-Sep-95	572	491	31	5.4	47	8.3	2	0.4	0	99.6
31-Dec-95	738	661	11	1.5	65	8.9	1	0.1	0	99.9
31-Mar-96	731	687	9	1.2	29	4.0	7	1.0	0	99.0
30-Jun-96	498	426	5	0.9	56	11.2	11	2.6	112	97.4
30-Sep-96	810	670	103	12.7	29	3.5	8	1.0	0	99.0
31-Dec-96	1062	953	59	5.6	41	3.9	9	0.9	0	99.1
31-Mar-97	1205	953	162	13.5	83	6.9	8	0.7	0	99.3
30-Jun-97	1366	1241	89	6.5	26	1.9	10	0.7	0	99.3
30-Sep-97	1838	1322	9	0.5	234	12.7	273	17.4	0	82.6
Total	16381	13666	955	6.0	1272	7.9	489	2.4	208	97.6

Note : Total percentages are averages of quarterly figures.

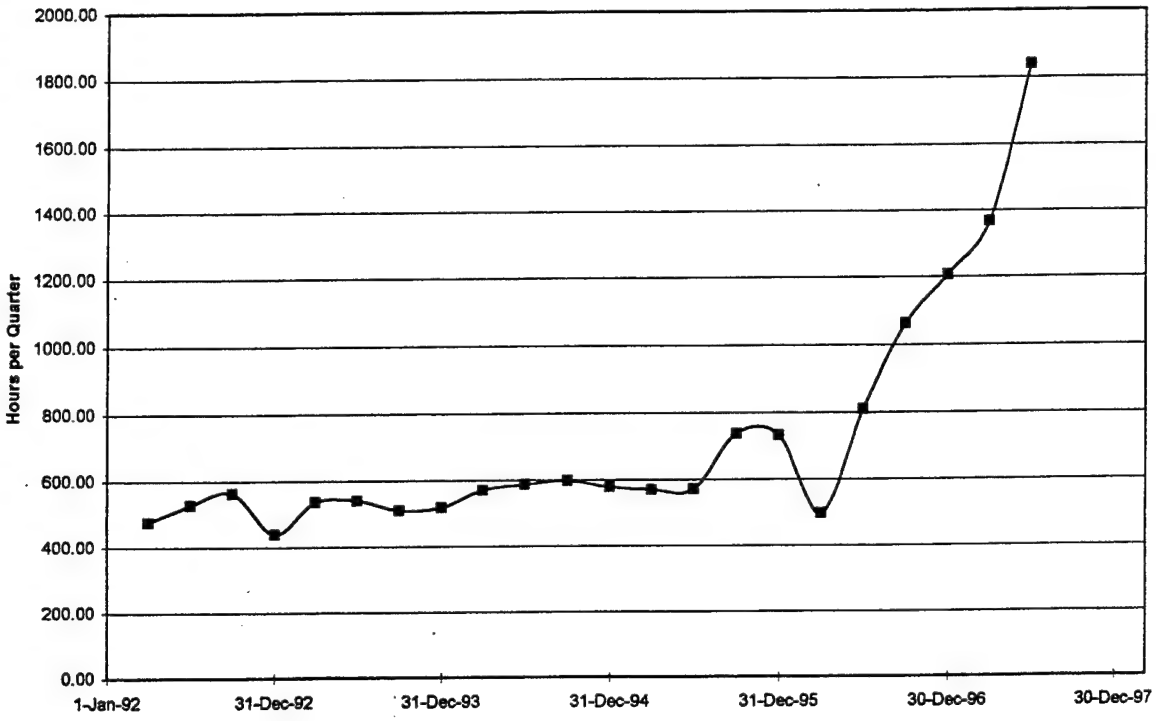


Figure 25. Scheduled Time by Quarter

5.2 SVGL Aligner Evaluation

5.2.1 Operation at Small Gap

Activities are underway to assure robust operation at small gaps. This work includes completion of wafer particle detection system (PDS) and qualification of an X-ray Image Sensor (XrIs) with no surface irregularity greater than 5μ, and implementation of software which assures gap uniformity and mask protection, and integration of small gap operation under run. The PDS hardware has been installed in the aligner and is being tested. The backup XrIS was laser-cleaned and has been installed into the aligner. It has been calibrated and qualified for use at 15μm gaps. Mask and wafers have been cleaned, inspected and qualified for small gap exposures. Other software upgrades include leveling and mask protection at smaller gaps.

5.2.2 Mask-Wafer Attraction (Charging)

Investigations have continued into the occurrence of mask-wafer attraction which can cause "crashes." This includes work on the new plan-of-record x-ray masks (SiC/Ta). Careful measurement of the properties of the mask showing evidence of attraction have been done.

Scratches and other evidence of contact have occurred sporadically during recent pilot line applications which still use the gold absorber masks. Masks from this application have been characterized for membrane stress and for topography. The stress was within specification but one mask had significant deformation in the non-membrane area which could lead to contact. Gap-related system specifications will be re-analyzed and surface topography more carefully tracked to assure that only masks with acceptable topography are used. Activities were initiated to incorporate grounding of high absorber masks to reduce the charging. Because the SiC currently used is not conductive, contact to the absorber through the Cr etch-stop layer under the Ta must be used. An experimental procedure has been identified to measure relative photoelectron generation from the surface of x-ray masks. The procedure has been implemented to study x-ray masks with the latest process-of-record materials.

5.2.3 Throughput

Beamline control and communications were identified as contributing to excess overhead time during exposure. Improvements were made to make this overhead negligible so that the overhead between fields is limited to aligner step and settle time of <0.5 seconds. Throughput improvements have been completed to bring performance to 29 wafers/hour under benchmark conditions without degradation of overhead. Overheads have to be reduced an additional 34 seconds to reach the goal of 40 wafers per hour. Improvements have been identified which, when implemented, can reach this goal.

5.2.4 Overlay

Overlay stability is tracked by a "daily" monitor. Aligner-to-itself overlay error has been demonstrated to be less than 40nm mean + 3σ. The performance of the current aligner has been modelled to be 35-38nm; this has been verified in practice.

5.2.5 Contamination

Contamination is tested by cycling wafers through the stepper and measuring their contamination levels before and after the runs. In general, no particles greater than 12μ are found but five to seven smaller particles are added each pass. The source of these is being investigated.

5.2.6 Applications Support

The ALF process-of-record used APEX-E resist at the start of the contract year. An AWLV (Across Wafer Linewidth Variation study done on APEX-E showed that AWLV for APEX-E does not vary significantly with feature sizes from 350-175nm. APEX-E has also been characterized for printing 100nm features. The dose latitude at 25μ mask-to-wafer gap is about 20% better than at a 40μ gap. The AWLV control is about 8-10nm. The APEX-E process was reoptimized early in this reporting period with about a 20% gain in sensitivity and no observable deleterious effects on contrast or

biases. Further work was done with APEX-E to develop an even faster process. Variables studied were post apply bake, post expose bake and develop time. A process was found that gave a sensitivity of 64mJ/cm^2 and an acceptable exposure latitude of ±16%. This was within the target range of 70mJ/cm^2 maximum. This is run #5 on the process matrix in Table 9. Figure 26 shows 175nm lines printed by process 5.

Table 9. APEX-E Process Parameters

Run Number	PAB (°C/seconds)	PEB time (min.)	Develop time (sec.)	Eo (mJ.cm^2)	Dnom (mJ/cm^2)	Exposure Latitude (±%)	D_{nom}/E_o
1	105/105	2	90	70	102	19	1.45
2	95/90	2	90	65	86	18	1.32
3	105/105	2.5	240	55	60	15	1.09
4	95/90	2.5	90	60	60	11	1
5	105/105	3	150	55	64	16	1.16
6	95/90	3	90	55	78	19	1.42
7	105/105	4	90	50	73	18	1.46
8	95/90	4	120	55	-	-	-

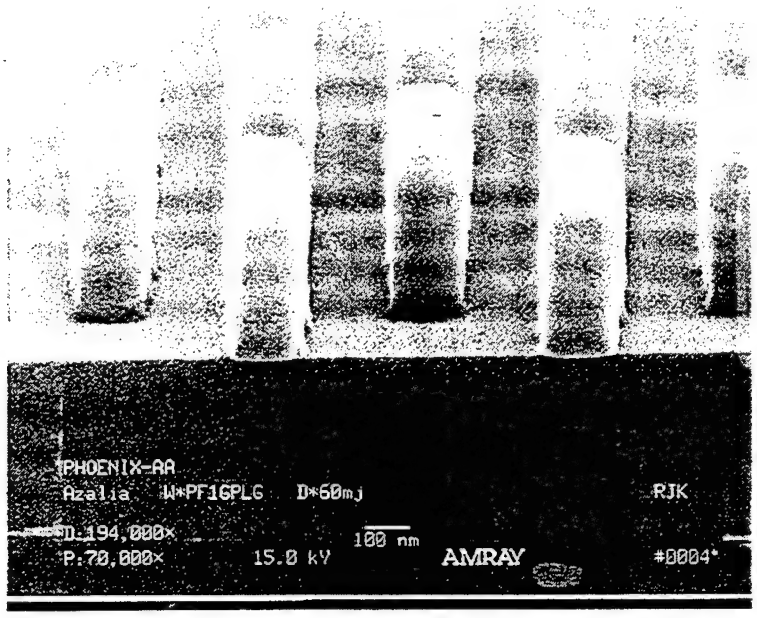


Figure 26. APEX-E Resist Process #5, 175&m.m Lines

Two other resists were also studied early in this period. TDUR resist from Tokyo Ohka Kogyo Co. was found to not warrant further investigation due to low x-ray sensitivity and small linewidth budget for isolated lines. The evaluation of a new IBM resist, UV-4, was started. This resist showed better isolated line performance than the previous UV2-HS. Samples were prepared with increased sensitivity, but these

showed decreased linewidth overexposure budget. The process development for UV-4 was deemed worth continuing. One hundred nanometer features were studied with high resolution mask LTM-4. Exposures were made on the SVGL stepper at gaps of 15, 20 and 25μ with APEX-E and UV-4 resists. The 25μ gap setting did not produce an exposure window to print 100nm lines with 1:1 line:space ratio. A small exposure window for nested lines was found at 20μ gap and it increases to 35mJ/cm^2 at 15μ gap. At 15μ gap, exposure latitudes for nested and isolated lines were $\pm$9% and $\pm$10%, respectively. APEX-E and UV-4 showed similar gap dependence. The print bias linearity of APEX-E and UV-4 were also similar. Figure 27 shows the excellent linearity for UV-4 for both isolated and nested lines. Figure 28 on page 57 shows resist images from this experiment.

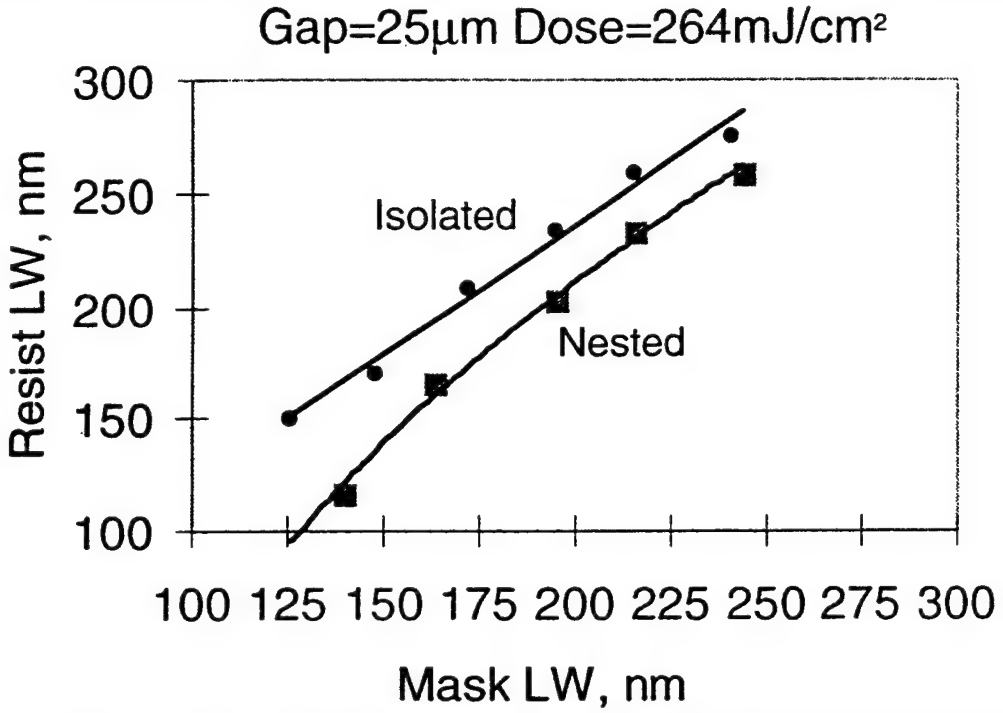


Figure 27. UV-4 Linearity

UV-4 resist was selected for the 1Gb test site program. Two grades of the resist were used for the process characterization to cover a total thickness range of 500 to 9500Å. For the 175nm critical dimension, UV-4 had $\pm$23% exposure latitude for contact holes, $\pm$13% for equal lines and spaces and $\pm$18% for 1:1.24 lines and spaces at 25μ gap. CD control for the active area level critical process was also confirmed with two lots of test wafers exposed a week apart. The wafers had a binodal CD variation which may have been related to the mask CD variation or to the PEB hotplate temperature variation. However, the CD variation meets the product specification. UV-4 reist is now the process-of-record for ALF.

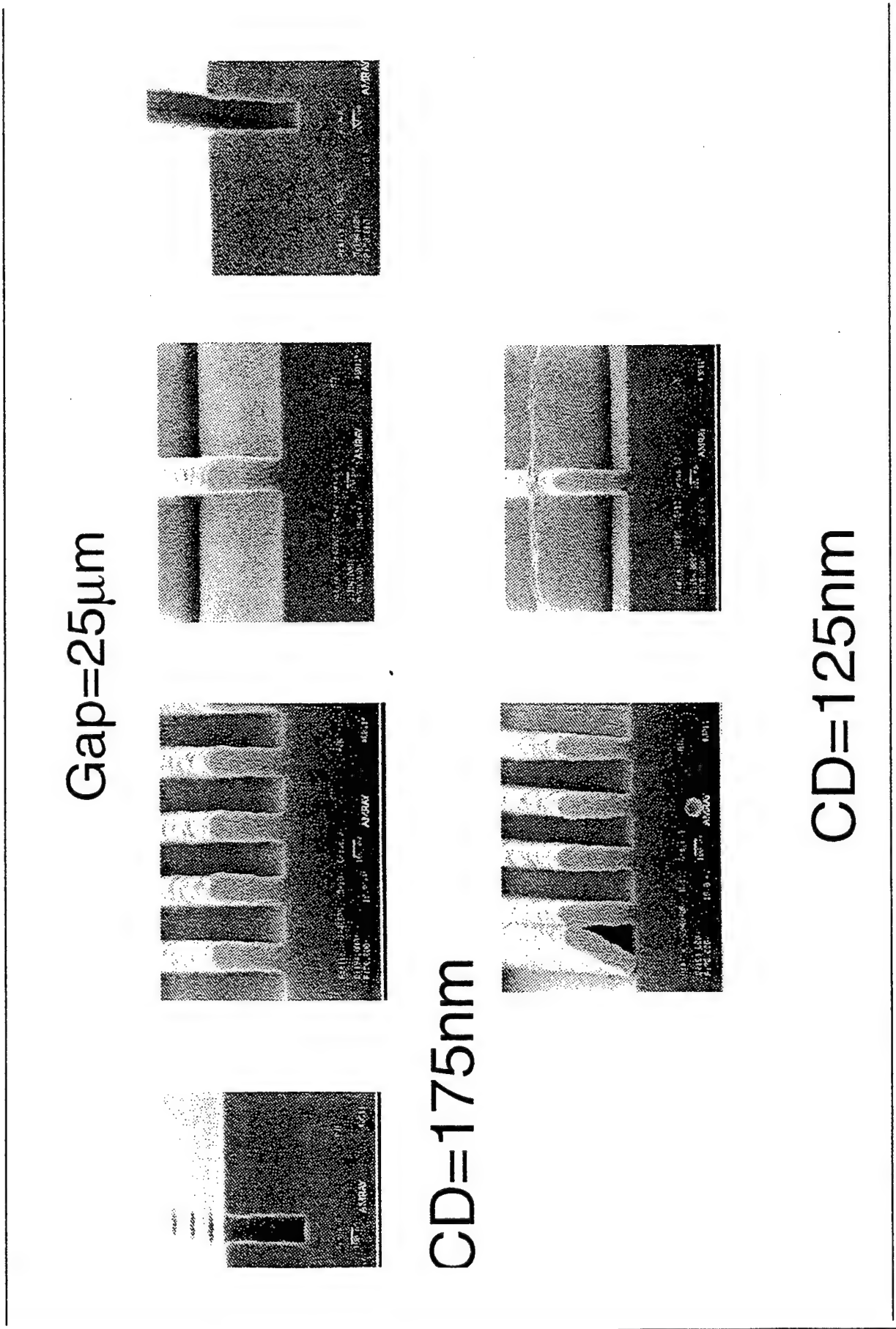


Figure 28. UV-4 Resolution Capabilities

As reported in the previous section, the scanning beamline mirror was replaced during March, 1997. To test the effectiveness of the new mirror, across chip linewidth variation (ACLV) has been measured using the NIGHTEAGLE pattern mask. The mask used had a gold absorber and a 5μ Si membrane. The chip size was 32×16mm. The ACLV measurements were made on wafers printed with APEX-E photoresist. Measurement sites were located on a 2×2mm grid with 12 measurements. Four chips were measured on four wafers. ACLV on the wafers was only slightly larger than on the mask. The small differences may be caused by statistical noise. An F-test applied to the ACLV measurements showed that the differences in variances between the mask and wafer are not statistically significant. The conclusion is that the new mirror is not contributing to ACLV and the installation is, therefore, successful.

As part of this study, an error budget analysis for ACLV was undertaken. Exposure control (dose uniformity and gap uniformity) and resist bake uniformity were considered to be the major contributors to linewidth print error. Estimates of exposure and reist error contributions were made using established values for the individual contributions. The conclusions were that mask ACLV dominates with 82% of the budget, followed by resist with 16% of the budget, and exposure at 2%, the smallest contributor to ACLV, as shown in Figure 29.

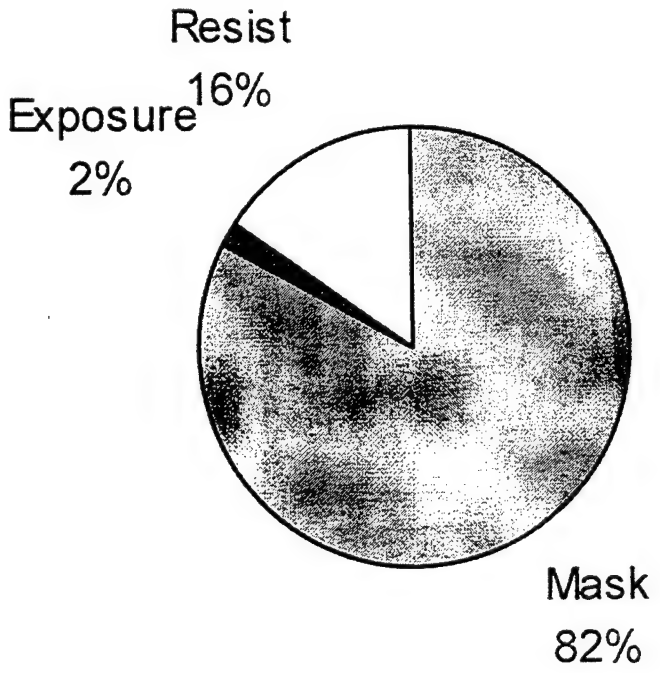


Figure 29. ACLV Error Budget of Variances

UV-5, a new positive, chemically-amplified resist of the ESCAP family, was also characterized. It was exposed on the Suss stepper at 25μ gap with 175nm isolated and nested lines. UV-5 has higher sensitivity than the UV-2 or UV-4 resists. Exposure latitude for nested lines is better than UV-4 (14% versus 10%) and nested to isolated

bias is significantly better (41nm versus 25nm). UV-5 resist also has significantly improved PEB latitude compared to UV-4. Table 10 and Table 11 show the effects of post-apply bake, post-expose bake, and nested and isolated lines, respectively, for UV-5.

Table 10. Effect of PAB and PEB on Clearing Dose

	PAB °C	PEB °C	Do, mJ/cm²
Wafer #1	*135*	*140*	*150*
Wafer #2	*140*	*140*	*130*
Wafer #3	*135*	*145*	*140*
Wafer #4	*140*	*145*	*130*

Table 11. Exposure Latitude for Nested and Isolated 175nm Lines

	Dnom, Nested (mJ/cm²)	Dnom, Isolated (mJ/cm²)	Exposure Latitude Nested (%)	Exposure Latitude Isolated	Nested/ Isolated Bias
Wafer #1	*190*	*243*	*13*	*9*	*43*
Wafer #2	*187*	*238*	*14*	*9*	*41*
Wafer #3	*173*	*221*	*13*	*7*	*56*
Wafer #4	*169*	*215*	*11*	*7.2*	*52*

The MMD has switched from Au on Si masks to refractory metal on SiC. A refractory metal/SiC NIGHTEAGLE pattern mask was received from the MMD and characterized for ACLV with APEX-E, UV-4 and UV-5 resists. The average critical dimension (CD) variation for 128 sites on four chips per wafer was 13.3nm 3σ with the mask variation included, and 9.8nm residual with the mask contribution removed. The residual seems to be larger than previously found for Au masks (9.8nm) Investigation of CD error sources will continue.

5.3 Process Development

5.3.1 Negative Resist Process

A negative, chemically amplified resist, CGR2205 (manufactured by IBM), has been installed at ALF. The resist was formulated to produce a coated film in the 4000 - 6000Å thickness range. The resist was used to optimize a gate level of IBM's CMOS-6X logic product for x-ray lithography. The feature to optimize was 190nm isolated line in resist.

Design of experiment (DOE) was done to determine resist sensitivity to exposure and process parameters. The DOE was done in two steps the goal of the first step was to maximize the exposure window; in the second step, the best process was chosen using exposure latitude (linewidth change with the exposure dose) as a primary response parameter.

The x-ray mask with SiC membrane and TaSi absorber had a negative tone and a contrast of 3.7 according to TRANSMIT simulations. That means that, at higher doses, resist will start cross-linking in shadowed areas resulting in scum and residual film in the areas that should be clean. Thickness of resist film as a function of exposure dose is shown in Figure 30. In this figure, squares represent thickness of developed resist that had been exposed under SiC membrane. The diamond curve represents resist thickness attained under absorber exposure. The gel points for resist exposed under SiC and TaSi are 36mJ/cm^2 and 136mJ/cm^2, respectively, with good correlation to the simulated contrast. The lithographically useful regime, exposure window, is bounded by a tolerable resist thickness loss on the small dose side and clean open fields on the high dose side. For a process used in Figure 30, this window lies between approximately 96mJ/cm^2 and 136mJ/cm^2. It was found that the exposure window is largest at lower bake temperatures: 40mJ/cm^2 for T=95°C and 20mJ/cm^2 for T=105°C. Thus, a temperature of 95°C was chosen for the next DOE step. Temperature sensitivity was 4.6nm per 1°C.

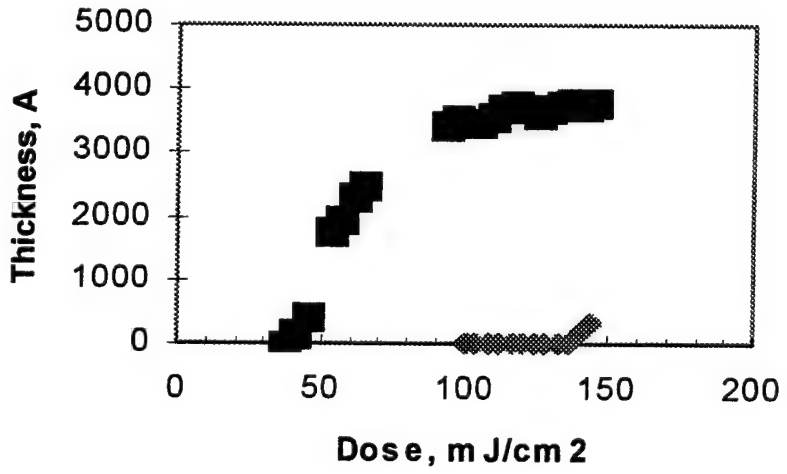


Figure 30. Resist Thickness versus Dose for CGR2205 Resist. (squares - resist exposed under SiC membrane; diamonds - resist exposed under TaSi absorber).

For the second step, exposure gap and post exposure bake (PEB) time were varied in 4×4 gap/bake matrix. Gap was varied from 15μm to 30μm (5μm step) and PEB time was 45, 60, 90 and 120 seconds. Gap sensitivity was 2nm per 1μm. The process chosen had an exposure latitude of $\pm$16.5% and the nominal dose of 78mJ/cm^2 (G=30mm, t=60 seconds). Spray7double puddle resist development was used, and the resist showed little sensitivity to development time.

Preliminary critical dimension (CD) control data shows chip mean variation across wafer in the range of 6-7nm with 12 chips per wafer, four wafers measured). This is consistent with the hotplate temperature control of $\pm$0.5°C and gap control of $\pm$1μm. Wafer-to-wafer mean CD stability was in the range of $\pm$4nm (five wafers exposed within five hours).

Further optimization of the process, including higher resolution patterns and studies of delay stabilities, are planned.

5.3.2 Lithography Characterization at 15μm Gap.

Exposures at small gaps are required for smaller groundrules. It was shown previously that 15μm gap is required for 125nm and 100nm features. The SVGL stepper was qualified for exposures at 15μm gap. Gap leveling was calibrated with the accuracy within 1mm in both *X*- and *Y*- directions. The UV-4 resist process was chosen as the process-of-record (POR) for this study. The process conditions are:

- Spin-coat at 5000 rpm to d0=4000Å.
- PAB at 135°C for 60 seconds.
- Expose at 15μm gap.
- PEB at 140°C for 90 seconds.
- Development: two spray/puddles for 30 seconds each (0.263N TMAH).

Mask LTM-5 #26B-6 (Si membrane of 5μm thickness + TaSi absorber) was used. One hundred and fifty nanometer isolated, 1:2 and 1:1 nested vertical and horizontal structures were measured. For dose wedges, one site per chip was measured. The measured linewidths show good linear dependence with dose, with some exception in extreme under-exposed and over-exposed regions (which may be related to line non-uniformity at the ends of process windows). Exposure latitudes are between $\pm$12% to $\pm$14% for various features. Mask measurements of corresponding features have been done and full analysis of CD performance is underway. Figure 31 on page 62 shows dose wedges for 150nm and 125nm vertical isolated lines.

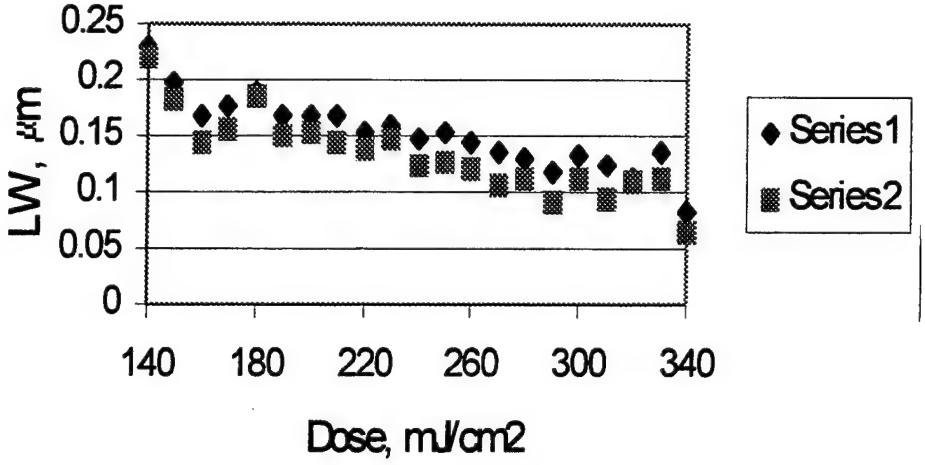


Figure 31. Linewidth Dependence on Exposure Dose. (verticalisolated lines at 150nm (diamonds) and 125nm (squares) nominal mask CD.

5.4 Contamination Control

5.4.1 Shipping and Handling

Early in this reporting period the mask shipping container was changed from the former "black box" to a special dedicated single mask SMIF pod with a special liner which was designed by the MMD. The goal is to ship and handle all masks in the dedicated SMIF pods. Several test shipments have been made from ALF to the MMD and back with no particulate adders on the mask. The ALF cleanroom was also upgraded with additional tool mini-environments, the conversion of ALF 1 stepper chamber to a clean wafer processing area, and an increased level of garmenting.

5.4.2 Protective Covers

The feasibility of a protective cover pellicle was previously demonstrated on the Suss stepper. Work was continued on protective covers for x-ray masks. Several types of PMMA, polyimide and SiN were tested but all failed radiation resistance tests. It was determined that a different type of mounting ring would be required for the SVGL stepper versus the one developed for the Suss stepper. Material and technique development are continuing.

5.4.3 Mask Cleaning

The ALF spot ablation laser tool (ASAT) is being used routinely to clean masks. Particles imbedded in the stack of wafers have also been successfully removed. The SVGL replacement XrIS was laser-cleaned to remove FM and features down to 5μ tall. The ASAT is capable of using the KLA SEMSpec coordinate system and is also capable of utilizing the ALF Inspex mask inspection tool coordinates. This allows FM found in ALF to be located in the ASAT and then removed. An IBM Europe-patented technique called laser steam cleaning (LSC) is also being investigated. Here, a thin layer of liquid is condensed on the mask or wafer surface. Then a laser pulse causes the liquid to explosively evaporate carrying away particles from the surface. The laser steam cleaning tool has recently been upgraded with a new chiller as well as an earlier thyratron replacement. Process development activities have resumed. Figure 32 shows a mask before and after LSC cleaning with 5μm foreign material removed.

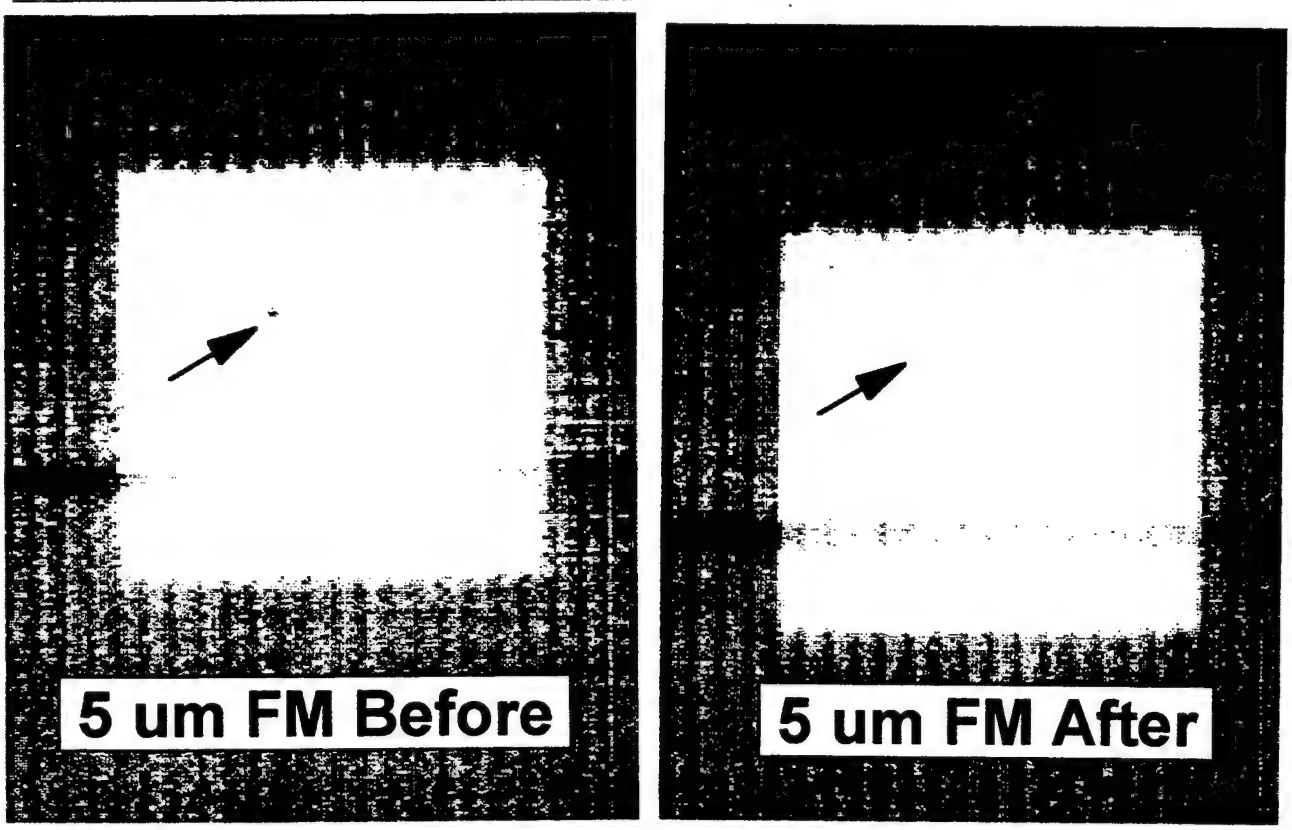


Figure 32. Mask Before and After Laser Steam Cleaning

5.4.4 Mask Lifetime

A mask lifetime study was started late in the contract period. The first part of this project was to process 3000 flop-down wafers through the SVGL stepper, measuring both the mask and selected wafers for added defects. This was planned as a second shift operation, but process and metrology problems delayed the job such that a

three-shift plan was implemented. A total of 3286 wafers were exposed with no light source downtime and an average stepper downtime of <45 minutes per day in a 12 day/24 hour per day marathon. The data is still being measured and analyzed.

5.4.5 Mask Transfer Robot

The mask transfer robot still has not been delivered but it is reported to be complete and operational.

6.0 Technology Acquisition (Task 8)

Task Objective: ***Evaluate the applicability and utility of new technology and tools to use in the MMD pilot production lines with the objective of improving production efficiency, quality, and profitability, and achieving progressively smaller mask feature sizes.***

The primary effort pursued during 1997 was the transition to a refractory metal process and the elimination of gold. Silicon carbide membranes were also implemented in conjunction with this transition. The work was completed three months ahead of schedule with the transfer from Task 8 to the process-of-record.

6.1 Silicon Carbide Status

During this contract period, HOYA shipped 762 silicon carbide films to the MMD. The foreign material on the films was measured both incoming and post clean. The average foreign material of the lot, as well as lot high and low, can be seen in SiC outgoing defects versus lot number Figure 33). The data collected is shown in Table 12 on page 66. Thickness has been within specification, but beginning with lot 51 the uniformity has increased due to measurement of a 50×50mm area. The previous area was 20×30mm. The samples that were scribed prior to film deposition were measured for film warpage and the film provides 3.23μm of warpage. The wafer warpage is included in the film warpage with all other samples. Figure 34 on page 69 includes a year of shipments and the film thickness, warpage and defects of those shipments.

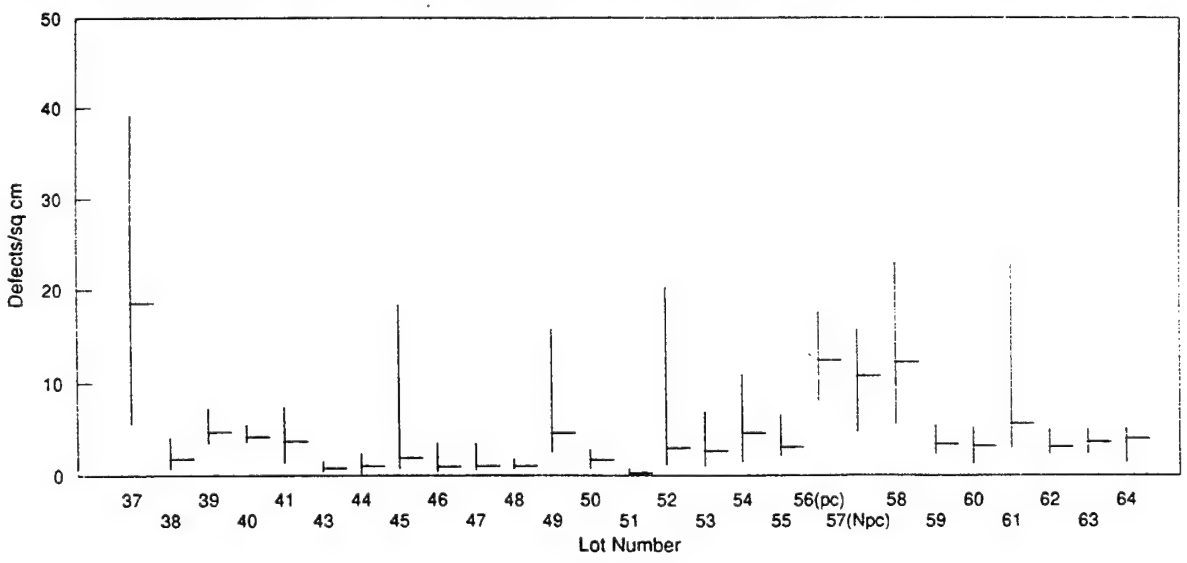


Figure 33. SiC Outgoing Defects

Table 12 (Page 1 of 3) Silicon Carbide Evaluation Summary

Date	Samples received	Incoming FM	Transmission optical HI MEAN LO	flatness: overall, membrane	thickness and uniformity	Image size	Image placement final	KLA	Comments
units	LOT(qty)	defx/cm²	%@=600nm	(μm)	(μm)	(nm 3σ)	(nm 3σ)	(defx/cm²)	
Target/ Spec		<1 of .5μ <5 of .2μ>	>50	<1.0	2.0±0.1 0.05	250,20	<50 X,Y	10 rprbl 0 non	
11/7/96	lot27(25)	(4.2)4.1 (51.2)51.6	54%	8.6	2.02 .015				backside/frontside issue..no scribe sent 100 unscribe (from 50X50) EM-2-1103C 5521706
11/7/96	Lot32(25)	(6.7)6.6 (9.3)8.7		8.6	1.99 .03				
12/5/96	Lot33(25)	(3.4).84		7.8	2.05 .0108				begins to meet FM spec sent 200 unscribed
12/27/96	Lot34(15) Lot35(15)	(14.2)17.8 (3.8)1.4 (33.7)18.2		8.7	2.07 .014				
12/27/96		(14.8)2.3 (115.2)17.9		7.8	2.08 .014				
1/21/97	Lot36(20)	(3.2) 2.3 (28.2) 4.1		10.6	2.01 .011				All meet .2μ spec sent 250 unscribed
2/7/97	Lot37(18) (12)	(5.4) 3.3 (161) 51.9		8.8	2.03 .012				with and w/out rejects
2/7/97	Lot38(25) (18)	(4.6) 2.6 (43) 17.9 (7.7) 2.4 (67.5) 43.6		11.4	2.02 .011				sent 25 litho-scribe plus 5 leica box
2/21/97	Lot39(25) Lot40(20)	(7.4) 1.8 (36) 10.2 (7.0) 4.7 (80.3)		6.4	1.99 .012 2.00H				9.36 H 0.3μm 4.595 H .5μm
2/21/97		(7.6) 4.5 (54.0)		7.4	2.02 .011				

Table 12 (Page 2 of 3) Silicon Carbide Evaluation Summary

Date	Samples received	Incoming FM	Transmission optical HI MEAN LO	flatness: overall, membrane	thickness and uniformity	Image size	Image placement final	KLA	Comments
		1.0μm sensitivity			50X50mm area				
3/14/97 3/14/97	Lot41(25) Lot42(25)	(3.2)3.1 (4.2)3.7		8.1 7.5	2.02 .031 1.96 .037				24 wfs each pulled 2 for warpage from 41
3/24/97 3/24/97	Lot43(25) Lot44(20)	(1.4)1.33 (1.2)1.1		10.2 12.6	2.07 .03 2.01 .03				24 wfs and 18 wfs for process pulled 3 for warpage
3/29/97 3/29/97	Lot45(25) Lot46(25)	(1.96)1.09 (0.91)0.96		9.3 13.6	2.02 .03 1.99 .03				24 wfs each
4/18/97	Scribe	(1.05)		3.23	2.02 .03				Flatness is DELTA to wafers stains etc.
4/18/97 4/18/97	Lot47(25) Lot48(20)	(1.38)1.05 (1.59)1.05		12.2 14.4	2.02 .03 2.00 .03				24/18 wfr
5/6/97 5/6/97	Lot49(25) Lot50(20)	(1.73)4.6t (.77)1.8t		12.6 11.6	2.03 .03 1.97 .03				24/24 wfr EM-2-1192C 5521842
6/10 6/10 6/10	Lot51(20) Lot52(20) 3.0μm	(1.58) (8.1t)1.69 (19.3)2.6t		8.02 11.0 8.76	2.09 .03 2.04 .03 2.93 .03				20/20 wfr EM-2-1260C 7520235
6/19 6/19	Lot53(25) Lot54(15)	(3.6)2.67 (5.9)4.6		10.05 9.69	2.02 .09 2.01 .12				40 of 50 EM-2-1260C 7520235
7/10 7/10 7/10	Lot55(10) Lot56(15) Lot57(16)	(9.66t)3.06t (20.5t)12.4 (33.67t)10.7		9.49 9.73	2.03 .04 1.958 .125r 1.976 .073r				regular prod no pre-cln cell pre-cln cell laser scribe

Table 12 (Page 3 of 3) Silicon Carbide Evaluation Summary

Date	Samples received	Incoming FM	Transmission optical HI MEAN LO	flatness: overall, membrane	thickness and uniformity	Image size	Image placement final	KLA	Comments
7/10 7/10	Lot58(12) Lot59(12)	(17.1t)12.2t (11.6t)3.4t		8.86 8.13	1.99 .033 2.02 .036				40 wafers this lot 14 used for exp
7/30 7/30	Lot60(18) Lot61(18)	(7.19t)3.2t (9.87t)5.6t		9.6 8.6	1.95 .035 1.99 .034				50 wafers this lot 14 used for exp
8/16 8/16 8/16	Lot62(24) Lot63(24) Lot64(18)	(63t)3.1t (45.1t)3.6t (297t)3.9t		6.1 7.6 10.0	1.97 .034 1.92 .032 1.93 .035				75 wafers this lot

Note: (as shipped defx) post meg clean "t" denotes new tencor data. "r" indicates range of thickness.

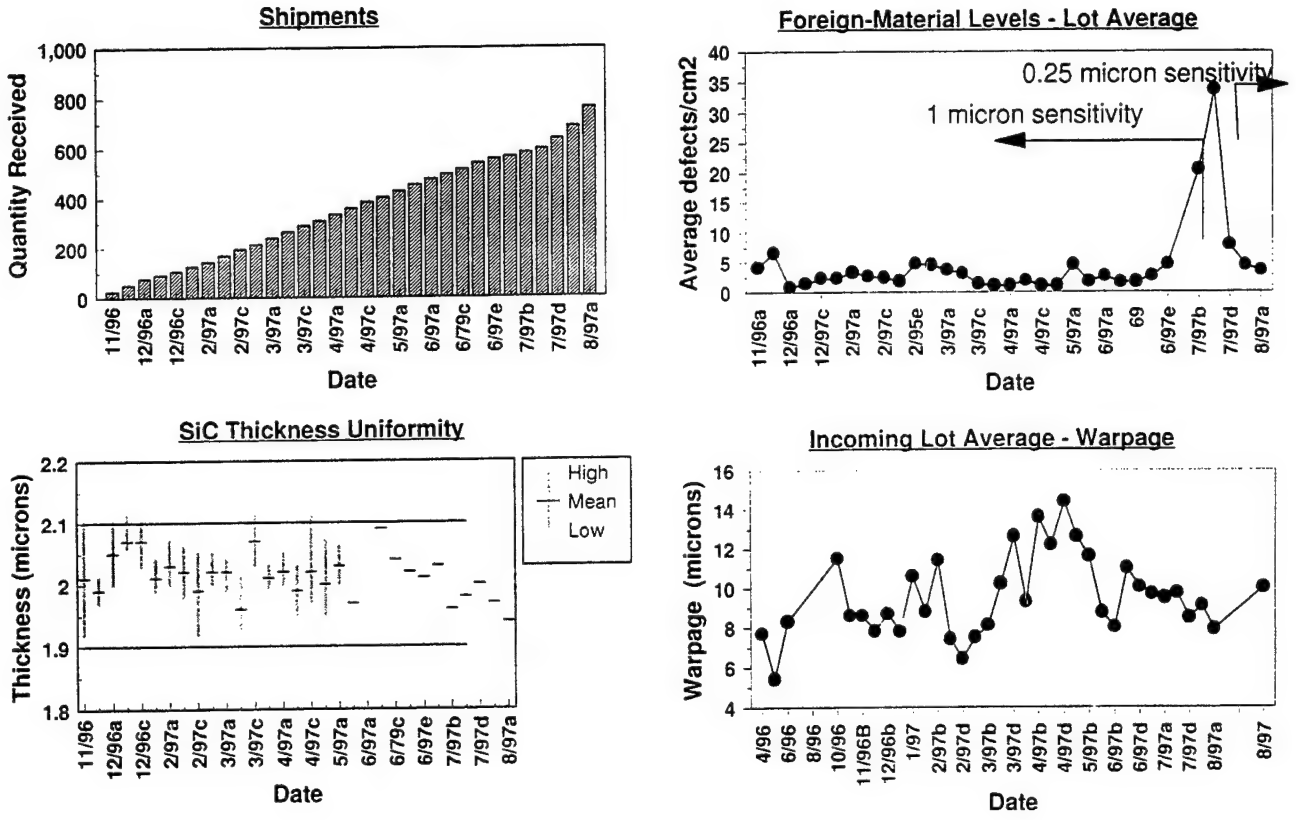


Figure 34. Silicon Carbide

6.1.1 Laser Scribe Wafers

Lots 56 and 57 were laser-scribed prior to shipping and the results indicate laser scribe at 3× the FM levels of litho-scribed parts. The laser-scribed wafers included a split between pre-clean and no pre-clean prior to silicon carbide deposition. The silicon carbide films were cleaned and inspected at Motorola for foreign material. The pre-clean cell averaged 10.7 (4.5 low and 15.8 high) defects/cm^2, while the no pre-clean cell averaged 12.4 (7.9 low and 17.6 high) defects/cm^2. Slightly cleaner films were found in the pre-clean cell; however, the films on the laser scribe parts were not as clean as the MMD litho-scribed parts, which average about 6.9 defects/cm^2, as measured in the silicon carbide films during the past year. At this time, MMD has no plans to pursue laser scribe.

6.1.2 Silicon Carbide Bubbles

There has been a lapse in SiC shipments due to a film problem that becomes evident during KOH (potassium hydroxide) membrane etch. The last shipment of 75 films was received on 16 August 1997. The silicon carbide bubbles up from the surface causing very small (0.1 to 10mm) defects ranging from two or three on a wafer to two or three

hundred. The process can be maintained by etching wafers in ethanolamine which causes no bubbles at this time, but does increase etch time by 3×. HOYA provided a matrix of the polishing process and wafer suppliers. HOYA and the MMD hope to find the cause of the bubbles by processing wafers from different suppliers through film deposition with and without polishing. The process matrix is shown in Table 13, and the results of the process can be seen in Table 14 on page 71 The three wafer types are listed at the top - IBM, HOYA-supplied wafers with flats and HOYA-supplied wafers. Wafers from each supplier were split into polished and unpolished cells. There were three wafers in each cell with the exception of the HOYA-supplied wafers with no flat. There were nine wafers in the HOYA wafer cell with no flat. The number of bubbles, the size and shapes were observed through a 2×2cm opening and the number of defects were then multiplied by the necessary number to obtain the total number of bubbles per wafer. The number of bubbles were counted on both the back and front of the wafers after KOH etch and are listed with the rows marked "F" and "B" in Table 14. There were some differences noted depending on the wafer type and polishing process. The IBM-supplied wafers had a greater range in the size of the bubbles. These bubbles average about 4-5mm in diameter. The Hoya-supplied wafers, both polished and unpolished, had smaller defects, but they were in greater numbers. The bubbles are usually round, but if the bubble breaks during the membrane etch process a small square or rectangular membrane will form. There are also triangular bubbles. The outside edge of the IBM wafer also etched, indicating possible damage during the deposition process.

Table 13. HOYA Process Matrix

	Plate No.	Wafer	SiC	Thickness	Rms
Case 1	*1* *2* *3*	*IBM* *IBM* *IBM*	*Unpol-ished* *Unpol-ished* *Unpol-ished*	*2.18* *2.17* *2.17*	- - -
Case 2	*4* *5* *6*	*IBM* *IBM* *IBM*	*Polished* *Polished* *Polished*	*2.02* *1.98* *1.98*	*0.56* *0.58* *0.37*
Case 3	*7* *8* *9*	*HOYA* *HOYA* *HOYA*	*Unpol-ished* *Unpol-ished* *Unpol-ished*	*2.18* *2.11* *2.12*	- - -
Case 4	*10* *11* *12*	*HOYA* *HOYA* *HOYA*	*Polished* *Polished* *Polished*	*2.02* *2.02* *2.03*	*0.65* *0.49* *0.74*

Table 14. HOYA Process Matrix Results

		IBM Polished	IBM Unpolished	HOYA w/Flats	HOYA w/Flats Unpolished	HOYA Polished
Number of Bubbles	*F* *B*	*6* *75*	*13* *70*	*37* *206*	*51* *150*	*35* *184*
Size Range (mm)	*F* *B*	*0.1-8* *0.1-10*	*0.1-10* *0.1-6*	*0.1-1* *0.1-1*	*0.1-3* *0.1-3*	*0.1-4* *0.1-6*
Average Size (mm)	*F* *B*	*4* *5*	*5* *4*	*0.75* *0.75*	*2* *1*	*2.5* *3*
Observed Shapes of Bubbles	*F* *B*	*Circle, edge damage* *Odd shapes*	*Circle, edge damage* *Odd shapes*	*Circle, rough wafer edge* *Odd shapes*	*Very small odd shapes* *Very odd shapes*	*Odd shapes, circle* *Odd shapes*

HOYA has several actions planned to eliminate the bubble problem:

- Tool cleaning frequency will be increased and fewer wafers will be run through the tool between cleans.
- Wafer position in the reaction tube will be optimized in relation to the gas inlet position.
- A flow rate study will be performed.
- A few additional wafers will be processed with extra polishing prior to deposition.

Along with polishing wafers to improve quality, HOYA will process a reduced number of parts while they attempt to solve the problems. The commitment has dropped from 100 films per month to 50 films per month.

Continued production of boron-doped silicon will allow the MMD to meet the need for substrates. One concern with continued use of boron-doped silicon is surface roughness. Boron-doped wafers measured by Atomic Force Microscopy (AFM) at IBM Yorktown Research are four to six times rougher than polished silicon carbide. Silicon carbide usually measures 5Å or less and boron-doped silicon measures 20-30Å in a 20×20μm area. Of seven wafers measured, three locations had large pits and trenches measuring from 170 to 360Å. The full impact of boron-doped silicon surface roughness is not fully understood, but it could impact the stress of deposited films -- and after SiON etch processing and resist strip the tantalum silicon surface becomes very rough. This has been associated with the CF_4 (carbon tetraflouride) added at 4% to the resist strip process. Processing of boron-doped silicon refractory films continues under engineering control.

6.1.3 HOYA

MMD met with representatives from Hoya to review plans for the continued cooperative effort between the two companies. Hoya plans to purchase a new CVD system which should improve yields, increase stress uniformity and reduce silicon carbide defects. Their target is to have this tool on line in 4Q97 and in full production by the end of 1Q98. Hoya agreed to reduce defect levels and to place special emphasis on the "glob" defects which are "mask killers." They have initiated a study of the cause and elimination of these defects. MMD and Hoya will work closely on problems through continued monthly telephone conferences. Hoya will report on their progress in 2Q98.

A purchase order was placed with Hoya Corporation for 1400 silicon carbide wafers to be supplied at the rate of 120 wafers per month for approximately one year. The current "interim" specification will be used with the exception of sheet resistance, <1000 ohms per square, which Hoya cannot meet. It was agreed to eliminate the sheet resistance requirement for the foreseeable future.

6.1.4 Crystallume

MMD has ordered fifty diamond films from Crystallume in Santa Clara, California. One of the considerations in obtaining films for membrane build from another supplier is the reduced availability of silicon carbide from Hoya due to the bubble problem. The properties of diamond was another consideration. Diamond has a very high Young's modulus, three times the modulus found in silicon carbide, which may help with image placement. There are, however, some issues to be addressed with diamond films. Surface roughness in the range of 50-200Å could make it difficult to control refractory film stress during deposition. Also, inspection systems such as the KLA see the roughness as a defect and make defect characterization difficult. Measuring image size becomes an issue as the system can be confused by the rough surface. The diamond films will be evaluated for surface roughness, film thickness, uniformity and stress.

6.2 Refractory Metal

As discussed earlier, the refractory metal deposition process has been successfully implemented. Several deposition processes are being developed at the MMD; however, to replace the processes currently being performed at Motorola. This will allow tighter process controls and quicker defect learning.

6.2.1 Refractory Metal Deposition

The x-ray refractory absorber deposition and annealing strategy described in earlier reports was partially implemented during 1997. The planned activities associated with accomplishing this were:

- Justification, purchase and implementation of sputter deposition system for chromium and tantalum silicon deposition - 2Q97.
- Justification, purchase and implementation of an automated stress measurement and mapping tool - 2Q97.
- Installation and calibration of borrowed AG610 annealing furnace.
- Evaluation of suppliers of new annealing equipment for 4Q97 justification and purchase.
- Evaluation of x-ray fluorescence as a nondestructive, rapid method measurement of chromium and tantalum silicon thickness.
- Justification and purchase of thickness measurement system - 1Q98.

In 1997, IBM approved $2.4M for the purchase and installation of a DC sputter deposition system for x-ray absorber films. The IBM Strategic Equipment Council approved the Sputtered Films Endeavor 8600 deposition system as "best of breed" for deposition of x-ray mask absorber films and this tool was selected for purchase on technical merit and price considerations. A purchase order was placed in June, 1997 and a commitment for delivery by 30 September was obtained from Sputtered Films. Factory acceptance was given on 29 September, the tool was delivered on 06 October, and installation was completed on 24 October 1997.

The deposition system consists of a central handler chamber, a load-lock chamber, an etch/degas chamber for wafer precleaning, a chromium chamber for etch stop mask deposition and a tantalum silicon chamber for x-ray absorber deposition. An option to provide SMIF capability for control of foreign material will be installed within six months of delivery.

Film depositions have begun and early data is promising. Deposited stress is repeatable at 222$\pm$3MPa. Films have been shown to anneal at 360-450°C depending on the initial deposition conditions (see Figure 35 on page 74). Film non-uniformity on a single wafer measured by resistivity is 0.44%, 3σ for average resistivity of 4.36 ohms/square.

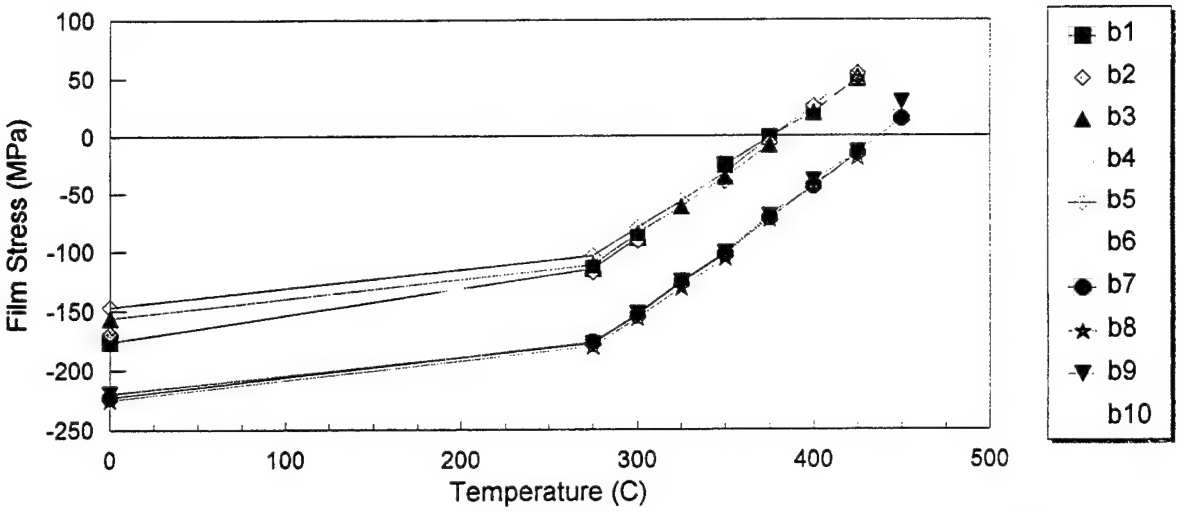


Figure 35. TaSi Film Stress

A Tencor 5510 stress measurement tool has been located in an IBM process area and is being utilized to support deposition and anneal process development. The MMD stress measurement system was ordered in September, 1997 and should be installed in February, 1998.

The AG610 furnace, on loan from IBM Yorktown, has been installed and calibrated and is performing very well. This tool will be used until a new annealing furnace is justified, selected and installed. Several suppliers were evaluated; Eaton Thermal Processing was the only one to quote $\pm 1°C$ temperature uniformity. The IBM Strategic Equipment Council has given preliminary approval for the Eaton Summit 200 Rapid Thermal Processing Furnace. Justification for $700K is proceeding for 4Q97 capital release.

Evaluation of x-ray fluorescence as a measurement technique for chromium and tantalum silicon films is ongoing. Two suppliers of x-ray equipment have shown that the technique works for both single films and the metal stack. Additional suppliers will be evaluated and justification will proceed during 1Q98. In the interim, thickness measurement will be done with profilometry; in-house x-ray equipment may be used as well.

6.2.2 Silicon Oxynitride Hard Mask Deposition

A new Plasmatherm SLR 730 PECVD System was purchased from Plasmatherm and installed in the MMD. This tool allows in-house capability to deposit both a SiON hard mask and a SiN sacrificial layer. The system includes a load-lock chamber and a plasma deposition chamber and is capable of processing four wafers (4-inch) at one time.

During the acceptance test in April, 1997 a series of deposition runs was performed to evaluate the tool performance. The properties tested included thickness uniformity, etch rates in KOH and HF, pinhole quality and film stress.

Upon acceptance of the tool, development work focused on optimizing the low stress deposition process for SiON. A set of depositions was performed with variations in N_2O and SiH_4 flows. Figure 36 and Figure 37 on page 76 show the effect of N_2O flow and SiH_4 flow on film stress. N_20 flows of 40 sccm and SiH_4 flow of 250 sccm give average stress values closest to zero. A process-of-record for SiON deposition has been established as follows:

250°C. electrode temperature
900 mT pressure
10 sccm NH_3
900 sccm N_2
40 sccm N_2O
250 sccm SiH_4 (2% in N_2)
7 minutes 20 seconds

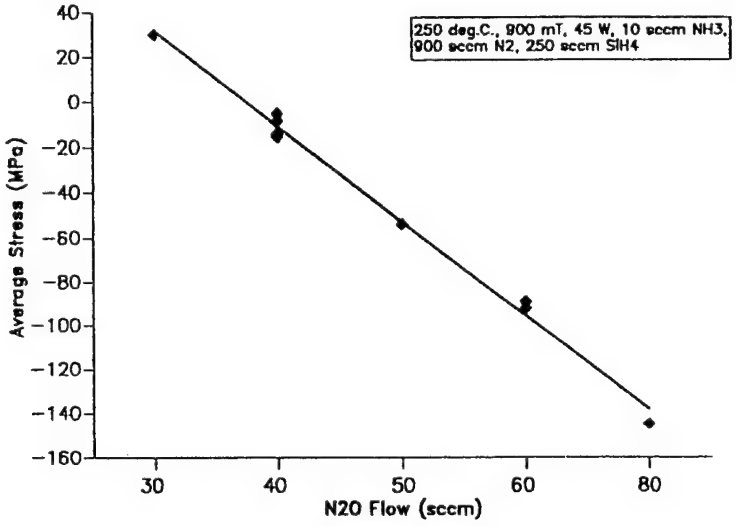


Figure 36. SiON Stress N2O Flow

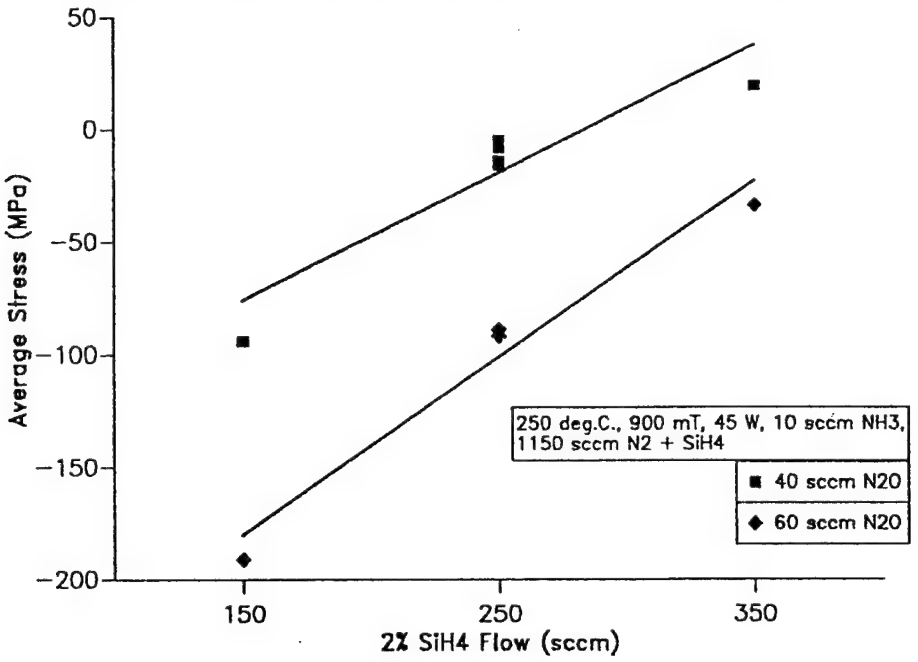


Figure 37. SiON Stress SiH4 Flow

Ten consecutive runs were performed with the process-of-record to check the repeatability of the thickness and stress (see Figure 38 and Figure 39 on page 77). The average thickness obtained with this process is 2005Å. Thickness uniformity and repeatability is within 2% in the membrane area. The average stress is -13Mpa. and is controllable within the repeatability of the measurement tool. Defect levels are typically very low with the deposited film having 5 to 6 large defects, most of which is FM that is removed during clean.

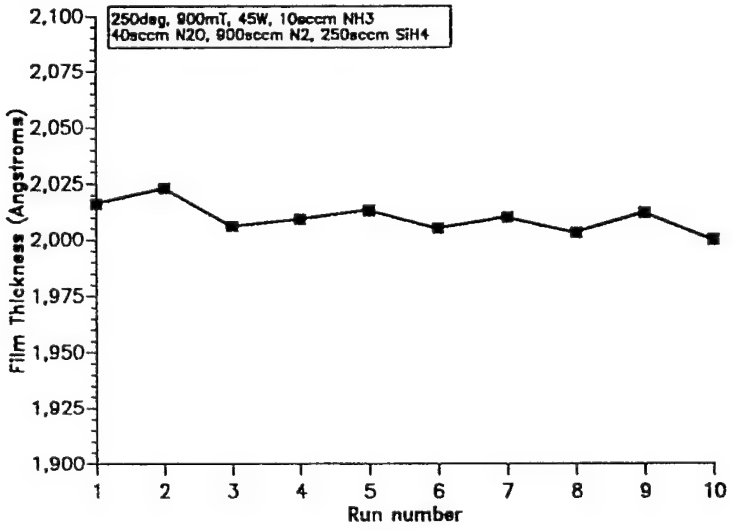


Figure 38. SiON Thickness

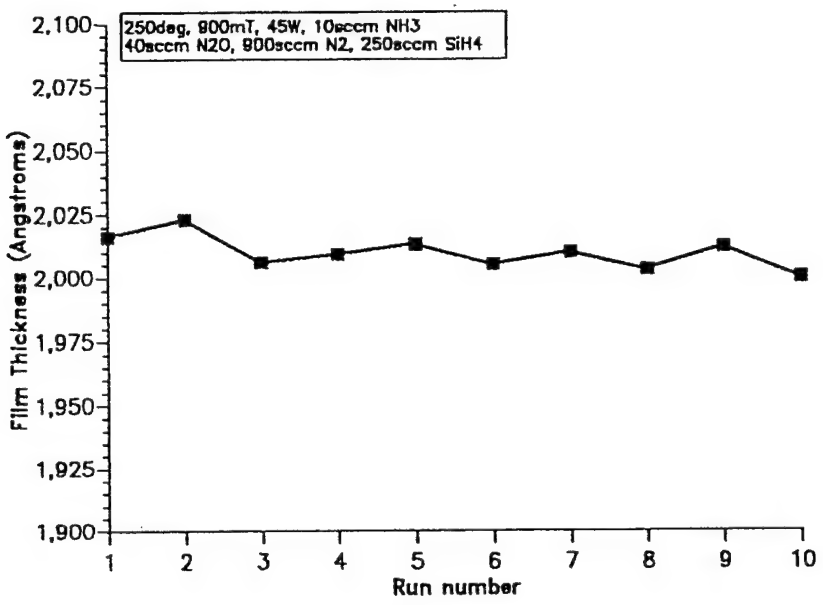


Figure 39. SiON Stress Repeatability

SiON films have been deposited on product quality wafers with the SiC/Cr/TaSi stack. The wafers are being processed through the rest of the line and made into masks. Etch behavior, image placement and final defect numbers will be closely monitored.

6.2.3 Refractory Etch

The transition to refractory technology required the development and implementation of a set of etch processes to pattern the absorber features. The process steps were developed to be compatible with the chosen SiC/Cr/TaSi/SiON refractory stack. During the first half of 1997 some of the process steps were transferred from Motorola PCRL to the MMD. In the latter half of the year, development work focused on qualifying and optimizing the etch process for both SNR and UVIII resists. In addition, several different product mask patterns have been etched.

The current implementation of refractory etch in the MMD consists of five separate process steps which are discussed in the following sections in sequence.

6.2.3.1 Resist Descum

Once the images have been defined in resist by e-beam exposure, bake and develop, a resist descum process is performed. This step is performed in a Plasmatherm 700 Series Batchtop Tool which is capable of holding four masks. An anisotropic descum process has been developed for the refractory masks at this stage. The process parameters are as follows:

25 sccm of O_2

20mT pressure (ignite at 50mT)
75W RF power
1 minute

Typically, up to 500Å of resist can be removed by this process, while there is a 10-20nm reduction in linewidth, dependent on feature size. The process works well on both SNR and UVIII resists.

6.2.3.2 SiON Hard Mask Etch

The SiON hard mask etch process has been qualified and is currently on-line in the MMD. A Plasmatherm System VII, capacitively coupled, parallel plate, plasma source tool is being used for this purpose. The initial transfer of the etch process from Motorola PCRL was completed in February, 1997. Qualification and optimization of the etch process for masks with SNR resist was completed by 2Q97, and the process was subsequently optimized for UVIII resist in 3Q97.

The current process of record is as follows:

350W RF power
20°C substrate temperature
20 mT pressure
1 sccm of O_2
7 sccm of CHF_3
20 sccm of Ar

An overetch of 40% past endpoint is used to clear the smaller features and compensate for the aspect ratio dependent etch (ARDE). Typical etch times are 6 to 7 minutes for SNR masks and 7 to 9 minutes for masks with UVIII resist. The etch rates of both resists is similar and roughly four times slower than the SiON. Typical etch bias data for both SNR and UVIII masks is shown in Figure 40 on page 82 and Figure 41 on page 83, respectively. The SiON etch process results in an image size-dependent etch bias, but for lines/spaces of 175nm, the bias is roughly less than 15nm on both SNR and UVIII parts.

6.2.3.3 Resist Strip

A resist strip process step has been implemented after the SiON etch. This process step is performed in a Plasmatherm SLR 770 Series RIE tool to remove all of the resist from the mask before proceeding with the final TaSi etch. Implementation of this resist strip step allows more flexibility with the resist thickness and reduces the aspect ratio for etching smaller features. It also eliminates any resist-dependent phenomena that may exist during TaSi etching. The current process-of-record involves nine minutes in a predominantly oxygen plasma. The process works well for stripping both SNR and UVIII resists. After the resist strip step, there is no observable effect on the SiON image size or quality.

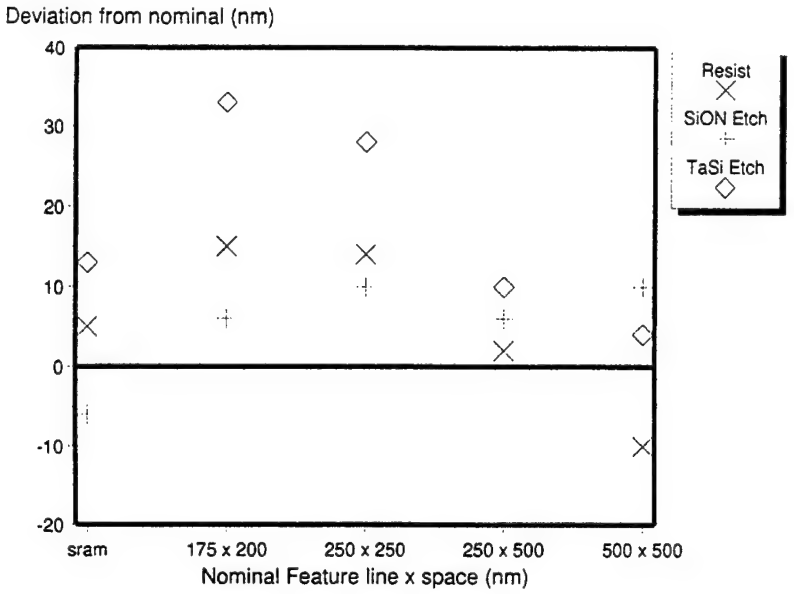


Figure 40. SNR Etch Bias Data

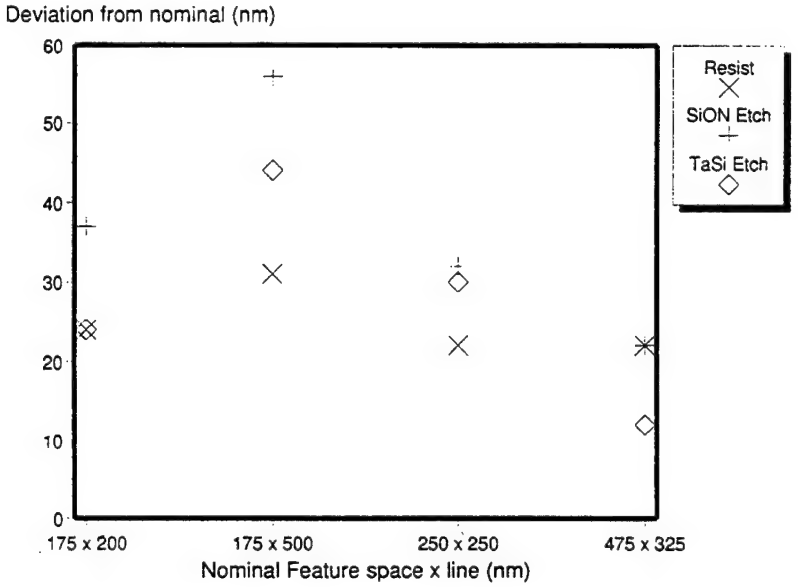


Figure 41. UVIII Etch Bias Data

6.2.3.4 TaSi Absorber Etch

The TaSi absorber etch process has been qualified and is on-line in the MMD. A Plasmatherm SLR 770 Electron Cyclotron Resonance (ECR) dry etch system is employed for this process step. The high density ECR plasma in this tool is better suited to etching refractory metals than conventional reactive ion etching tools. The TaSi etch process involves a chlorine gas chemistry and was initially developed by Motorola at their PCRL facility. The transfer of this process to the MMD was begun in late 1996 and continued through 1Q97. Optimization continued through 2Q97.

Initial process development work concentrated on an etch process for SNR masks, while later work involved developing a UVIII etch process. The process-of-record for SNR masks is as follows:

50W RF power
35°C substrate temperature
2 mT pressure
20 sccm of Cl_2
3.5 sccm of O_2

It is necessary to add oxygen during the etch to help sidewall passivation and reduce undercutting. Typical etch times are between 2 and 2.5 minutes, including a 35% overetch. It was also discovered during process development that the electrode-to-wafer gap is a critical dimension that affects the TaSi etch process. This gap has been reduced to 0.4mm from 0.8mm and, as a result, the etch process shifted to a more efficient regime. Future work will attempt to study this relationship in more detail. In any case, excellent results have been obtained in etching features 175nm and larger. Figure 42 on page 83 shows etched 175nm SRAM features from a NIGHTEAGLE mask. Some initial success has also been achieved in etching 125nm features as seen in the Viper mask in Figure 43 on page 84.

Good results have also been obtained in etching masks processed with UVIII resist. Initial development work on these masks has resulted in etch conditions similar to the SNR process, but at slightly higher power and substrate temperatures. Because of substrate shortages and product commitments, a full process development study has not yet been performed on UVIII masks. Nevertheless, several product masks have been processed and shipped. Image quality is good as shown in the 175nm lines and spaces in Figure 44 on page 84, and the 250nm features in Figure 45 on page 85.

In summary, TaSi etch processes are on-line for etching masks with 175nm and greater features from both resist types. The etch bias data is shown in Figure 36 on page 75 and Figure 37 on page 76, mentioned previously. Future development work will concentrate on improving etch processes for 150nm and smaller features.

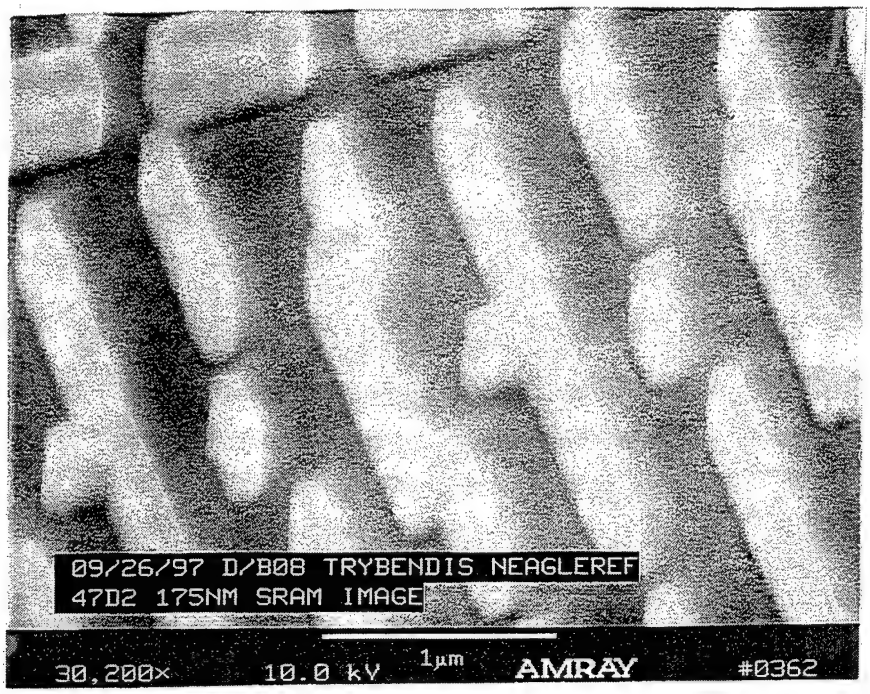


Figure 42. 175nm SRAM Line Monitor

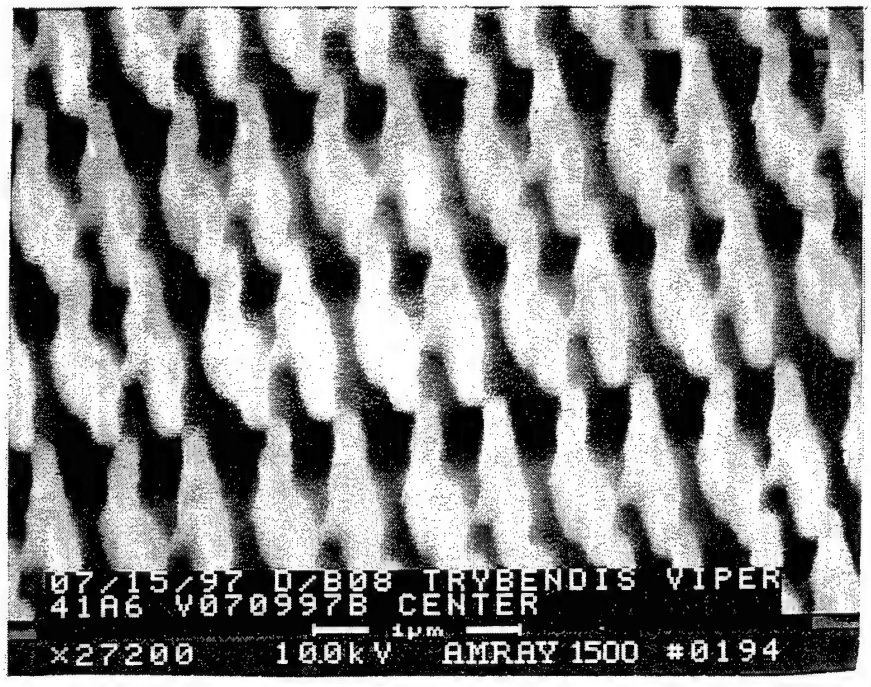


Figure 43. 125nm SRAM Line Monitor

6.2.3.5 SiON Hard Mask Strip

As a final process step after TaSi etch, it is necessary to remove the residual hard mask layer. This process step is still under development, and current studies are aimed at optimizing the strip process so that it has little or no effect on the quality of the final mask, which includes image size, placement and defects.

6.3 Proximity Correction Algorithm Evaluation and Optimization

A Technology Assessment Report was submitted on January 6, 1997 (reference CDRL G004, 97-MMD-LMFS-00002). This report discussed the results of optimization of the algorithms for the PMMA/gold process completed during 1996. The SNR/refractory process was optimized in the same way.

Testing of the DOSE6 software for the more-than-two Gaussian approximation highlighted a software functionality problem. This was corrected during the second quarter, and testing was initiated during the third quarter. The following conditions were evaluated and shown in Figure 46 on page 85 and Figure 47 on page 86 (all for SNR/refractory):

XE 2G Cur: DOSE5XE algorithm with two Gaussians using the current process-of-record parameters

D6 2G Cur: DOSE6 algorithm with two Gaussians using the current process-of-record parameters

D6 2G New: DOSE6 algorithm with two Gaussians using parameters predicted by simulation at IBM Yorktown

D6 3G: DOSE6 algorithm with three Gaussians using parameters predicted by simulation at IBM Yorktown

D6 6G SmlB: DOSE6 algorithm with six Gaussians using parameters predicted by simulation at IBM Yorktown

D6 6G LrgB: DOSE6 algorithm with six Gaussians using second set of parameters predicted by simulation at IBM Yorktown

A comparison of run times (all on the Parallel Post-Processor) is shown in Figure 46 on page 85. The DOSE5XE and DOSE6 cases with the same number of Gaussians and same parameters gave similar results, as did the DOSE6 three-Gaussian case. The six-Gaussian and new two-Gaussian cases produced run times that were two to three times longer. The cause of this is being analyzed, but it appears to be related to the value of specific proximity correction parameters.

A comparison of the dose assignments of multiple image types is shown in Figure 47 on page 86. The DOSE6 results are similar to, and in some cases better than, the DOSE5XE results. This is encouraging because the DOSE6 algorithm uses two less

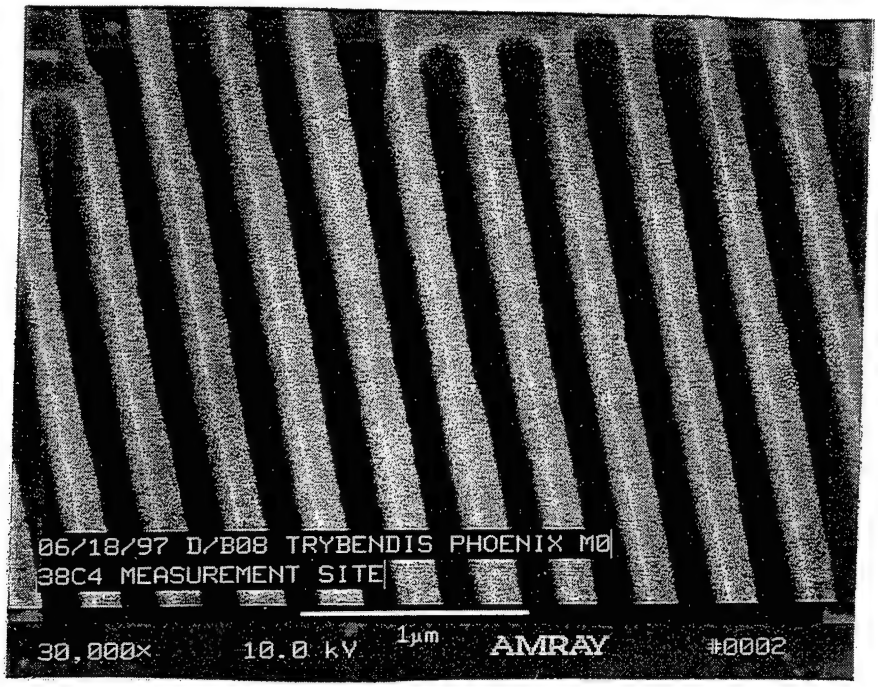


Figure 44. 175nm Space/Line

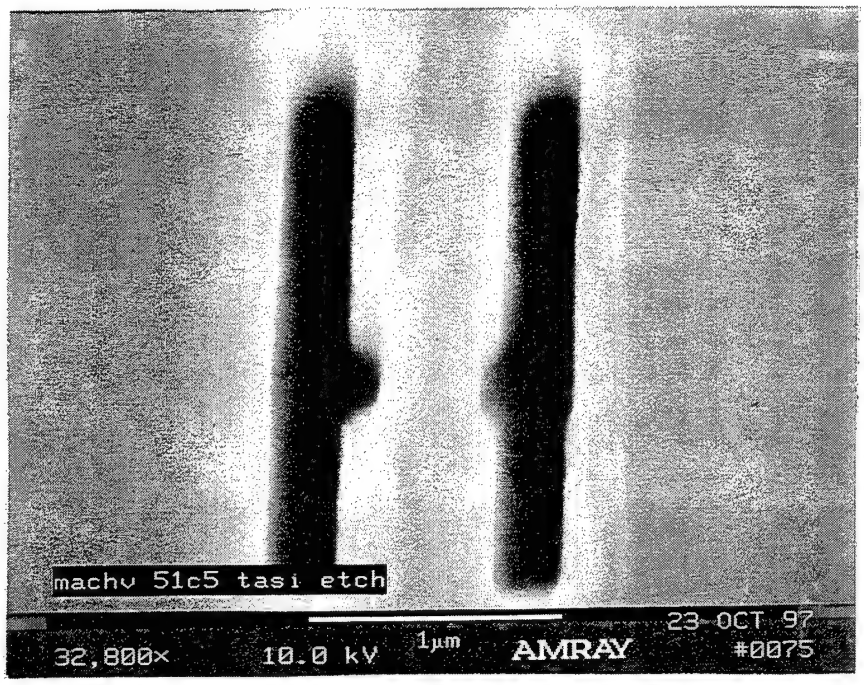


Figure 45. 250nm Feature

6.2.3.5 SiON Hard Mask Strip

As a final process step after TaSi etch, it is necessary to remove the residual hard mask layer. This process step is still under development, and current studies are aimed at optimizing the strip process so that it has little or no effect on the quality of the final mask, which includes image size, placement and defects.

6.3 Proximity Correction Algorithm Evaluation and Optimization

A Technology Assessment Report was submitted on January 6, 1997 (reference CDRL G004, 97-MMD-LMFS-00002). This report discussed the results of optimization of the algorithms for the PMMA/gold process completed during 1996. The SNR/refractory process was optimized in the same way.

Testing of the DOSE6 software for the more-than-two Gaussian approximation highlighted a software functionality problem. This was corrected during the second quarter, and testing was initiated during the third quarter. The following conditions were evaluated and are shown in Figure 46 on page 84 and Figure 47 on page 84 (all for SNR/refractory):

XE 2G Cur: DOSE5XE algorithm with two Gaussians using the current process-of-record parameters

D6 2G Cur: DOSE6 algorithm with two Gaussians using the current process-of-record parameters

D6 2G New: DOSE6 algorithm with two Gaussians using parameters predicted by simulation at IBM Yorktown

D6 3G: DOSE6 algorithm with three Gaussians using parameters predicted by simulation at IBM Yorktown

D6 6G SmlB: DOSE6 algorithm with six Gaussians using parameters predicted by simulation at IBM Yorktown

D6 6G LrgB: DOSE6 algorithm with six Gaussians using second set of parameters predicted by simulation at IBM Yorktown

A comparison of run times (all on the Parallel Post-Processor) is shown in Figure 46 on page 84. The DOSE5XE and DOSE6 cases with the same number of Gaussians and same parameters gave similar results, as did the DOSE6 three-Gaussian case. The six-Gaussian and new two-Gaussian cases produced run times that were two to three times longer. The cause of this is being analyzed, but it appears to be related to the value of specific proximity correction parameters.

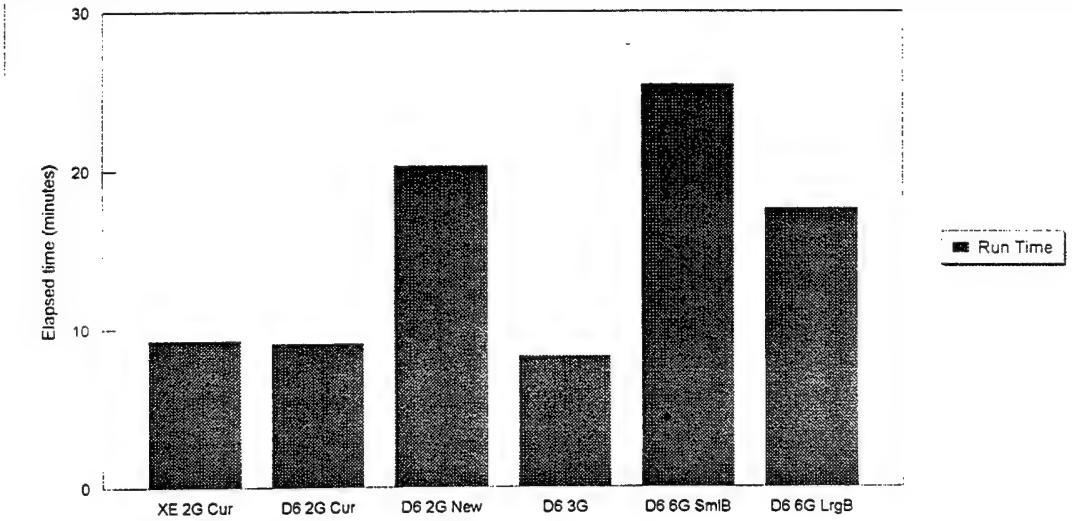


Figure 46. Run Time Comparison

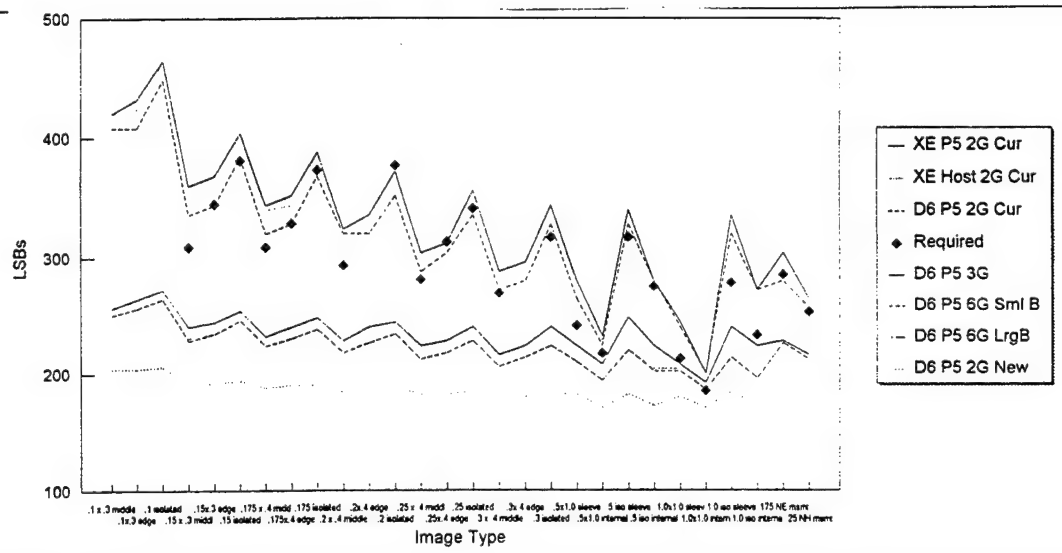


Figure 47. Dose Comparison

A comparison of the dose assignments of mulliple image types is shown in Figure 47. The DOSE6 results are similar to, and in some cases better than, the DOSE5XE results. This is encouraging because the DOSE6 algorithm uses two less variables to get this result, enabling a simplified optimization matrix. DOSE5XE has two 'non-proximity' variables which affect the results and must be optimized with the classic proximity correction parameters (reference Technology Assessment Report CDRL G004, 97-MMD-LMFS-00002).

The results from the parameters predicted by simulation were disappointing and indicate that either the simulation needs to be modified or that proximity correction is being used to correct for more than just proximity effect. Additional testing is underway to determine experimentally the point-exposure distribution. We would like

to determine close starting points for the more-than-two Gaussian cases to allow efficient centering of the optimization matrix.

6.4 Conductive Polyaniline

Work with the conductive topcoat, polyaniline, involved three major efforts throughout the contract period: 1) completion of the analysis started in 1996 with gold absorber masks and PMMA resist, 2) initial work with refractory stack masks with SNR, and 3) the resolution of filtration efforts.

The polyaniline topcoat showed significant improvement in both image placement and image size (multipass exposures) with PMMA resist. NIGHTHAWK test masks showed a 40% reduction in raw image placement (from $\simeq$90nm to $\simeq$50nm) with no PSE correction implemented at EL-4 P0. The topcoat also showed an improvement in repeatability. The best result from a NIGHTHAWK using PSE corrections was (27nm,21nm) while the best result from the control group was (27nm,31nm). Due to the fact that these masks were written with multiple passes, an image size variation performance improvement was also seen. The average 3σ value seen with the topcoat was 14.5nm, while the control group averaged 17.0nm. The best result seen on a NIGHTHAWK to date in the MMD, 11nm, was on a part using the topcoat. These benefits were seen on parts exposed with both the 3% (coated to 900Å) and the 5% (coated to 2000Å) formulations.

In the second half of the year, work shifted to assessing the feasibility and benefits from this conductive topcoat with SNR200 resist. Initial work involved both gold and refractory masks. Because SNR200 is a lower dose, chemically amplified resist with write times one-fourth of those seen with PMMA, charge characteristics were different. Also, the current process online is single pass and this was the process used for polyaniline analysis. Therefore, image size variation results were similar to those seen without the topcoat.

It was found that the compatibility and shelf life of the polyaniline with the SNR200 was much less stable than the PMMA. Therefore, studies involved different pH levels (2, 3 and 5) and different polymer concentrations (3% and 5%). Also, exposures were completed on the same day as the polymer was coated. Image placement results were much less conclusive than for the PMMA. NIGHTEAGLE masks written with no corrections (PSE) averaged 35-40nm with all different formulations of polymer and with the controls. Although the image placement character was slightly different for the 5% formulation, no repeatability improvement was found. The benefits of the polymer will be re-evaluated when multipass writing analysis begins in the first quarter of 1998 with UVIII resist.

The MMD installed a NOWPAK of polymer on the Suss tool with a 0.1μm filter which immediately became plugged. Several filters were evaluated with varying materials and pore sizes. The MMD successfully filtered 3% polymer that was prefiltered by the

vendor down to 0.45μm versus a 0.20μm target. The 5% formulation would not filter to this level. Monsanto is continuing to work on the filtration issue with IBM Yorktown.

7.0 Technical Interchange Meetings (Task 10)

Task Objective: ***Conduct Technical Interchange Meetings (TIM) for industry and the government on a bimonthly basis.***

The following Technical Interchange Meetings were held during the Option 2 contract period.

- An Executive Review Meeting was held at Lockheed Martin, Manassas, Virginia on 10 December 1996. This TIM was the final Executive Review of the MMD "Option Year One" contract. The minutes of the meeting were submitted in accordance with CDRL H002, reference 96-MMD-LMFS-00092.
- An Advanced Cost of Ownership TIM was held on 22 January, 1997 in Fort Lauderdale, Florida. The objective of this meeting, which was a follow-up to the 22 August 1996 TIM held in Chicago, was to assess the current status of the cost-per-mask calculations being generated by the advanced mask technology community. The minutes of this TIM were submitted in accordance with CDRL H002, reference 97-MMD-LMFS-00022.
- A TIM, hosted jointly by Lockheed Martin, IBM, SAL and CxRL, was held at the SPIE 22nd Annual International Symposium in Santa Clara, California on 12 March 1997. The purpose of this meeting was to generate interest in using x-ray masks and to report on the status of x-ray mask-making production. The meeting was attended by invitees from various semiconductor and related technology companies. The minutes were documented and submitted in accordance with CDRL H002, reference 97-MMD-LMFS-00034.
- A TIM was held on 9 April 1997 at the Sanders facility in Nashua, New Hampshire. The minutes were documented in CDRL H002, reference 97-MMD-LMFS-00039.

  The objective of this meeting was to gain an understanding of the requirements of the Point Source Program and its dependencies on the MMD contract. Also presented were MMD's current processes and capabilities.

  The focus of this TIM was to highlight the source, alignment systems and stage projects underway (Phase I) and to discuss preliminary mask format and quantity requirements needed for the Point Source program. Phase I is considered the "development" stage of the contract. The "validation" stage, or Phase II, was also introduced in the overview presented by Sanders.
- A TIM was held on 22 May 1997 at the Lockheed Martin facility in Manassas, VA. Attendees included representatives from Lockheed Martin, IBM and the Government. The purpose of this TIM was to review the MMD's status as it transitions from the well established and understood gold absorber process on boron-doped silicon wafers to that of tantalum silicon on silicon carbide wafers. The minutes of the meeting were documented in accordance with CDRL H002, reference 97-MMD-LMFS-00060. 01 June through 31 August 1997.

- A TIM was held on 24 June at the IBM Burlington, Vermont facility to discuss the merits of potential techniques to correct the magnification mismatch between the respective mask and wafer patterns for proximity x-ray lithography. The meeting was intended as a forum for discussion of the currently known techniques for providing magnification adjustment between mask and wafer, and to evaluate their respective merits. A complete report of the meeting was submitted in accordance with CDRL H002, 97-MMD-LMFS-00056, dated 08 July 1997.
- An Executive Review meeting was hosted by Lockheed Martin at the IBM Burlington facility in Essex Junction, VT on 25 June 1997. A System Design Review for the 0.13μm mask fabrication and a Critical Design Review for the 0.25μm mask production were held following the Executive Review. All materials presented at these reviews were distributed at the meeting. The meeting minutes are documented in CDRL H002, 97-MMD-LMFS-00055.
- An MMD Executive Program Review was held jointly with the SIA Lithography Technical Working Group Critical Review of X-ray Lithography. The meeting was held on 22 October 1997 at the IBM East Fishkill facility in Hopewell Junction, New York. Attendees from industry and the government participated. Reference CDRL H002, 97-MMD-LMFS-00084.

Appendix A. IBM Yorktown Summary

Variable Shaped Beam E-Beam Post Processing

Historically, all post-processing of mask patterns for the e-beam mask writer has been done on large mainframe computers in central data centers. However, this approach has several practical drawbacks, which have become increasingly significant as data sets become larger and more complex:

- Only a fraction of the mainframe's CPU time is available, and the actual elapsed time to process a large data set can be unpredictable as well as long.
- The amount of data storage is also limited, which has prevented processing of the larger data sets without breaking them up into pieces.
- The recurring costs of processing data in the data center are growing increasingly large.
- The outlook for commercialization of e-beam systems requires that post-processing capability be delivered with the tool, which virtually requires a stand-alone post-processing system.

To deal with these issues, a project was initiated to port the post-processor code from the mainframe to an IBM RISC computer platform with parallel processing. Such a porting would have a number of advantages:

- Post-processing could be done on a dedicated system, eliminating the dependency on and costs of the data center. A dedicated system makes it easy to provide commercialization, and the cost savings are expected to cover the capital cost of the system in a relatively short time.
- The storage capacity can be increased almost arbitrarily by adding storage modules, as required.
- The computational speed can be enhanced by increasing the number of parallel processors, as required.

To realize such benefits, a major project was undertaken to implement Parallel Post Processing capability for the X-Ray Mask Maker (XE-P0) on the IBM SP computer. The SP is currently configured with six nodes and has expansion capability to 512. The new post-processor is known as P5 (**P**ractically **P**erfect **P**arallel **P**ost-**P**rocessor).

The first phase of the project consisted of porting the existing code off of the mainframe and onto the IBM RISC platform. There are several programming languages employed by the Post-Processor. Most had counterparts on the RISC. Those that did not had to be rewritten. In addition, the I/O service software and all interfaces to the Sorting Program Product had to be replaced.

After thoroughly testing the "Serial" version of the RISC based Post-Processor, the Parallel code, which was developed during the port phase, was integrated and tested on the IBM SP computer. There are a total of 250 KLOCs of source code in the entire software system. About 40% of this code had to be modified for the project.

The last phase of the project consisted of the following items:

1) Final software reconciliation with the host (mainframe) version
2) Definition and execution of the qualification test with the customer
3) Tuning of the system for optimal performance
4) Freezing and release of the software to the customer

Since normal maintenance activity occurred during the life-cycle of this project, a final reconciliation of all enhancements and fixes had to be merged into the Parallel software prior to the qualification. This was accomplished and the resultant executable was successfully verified against a set of project test cases.

The qualification test consisted of one design, Plutus M1, posted for a positive tone (PMMA) resist and a second design, Phoenix DT (1Gb), posted for a negative tone (SNR) resist. Each of the designs was posted using both P5 and NPP (the Data Center version), written side-by-side on a ring-bonded membrane, and subsequently checked for differences using the KLA inspection tool. The qualification was completed with only minor issues, which were immediately resolved. The P5 software system replaced NPP on 3/25/97, ahead of schedule.

(It should be noted that the P5 post-processor can be used for the Hontas 6 and P0 variable shaped beam e-beam tools, but is not applicable to vector scan tools such as VS-5, which has a completely separate post-processor.)

Besides the obvious cost savings for the AMF, the P5 software on the IBM SP computer platform gives the AMF a dramatic reduction in elapsed time between the receipt of the design and the generation of 'tool ready' data. Table 1 indicates this savings across logic, SRAM, and DRAM technologies, where the NPP column indicates the time required using the data center. All data in the table come from real processing runs.

Table 1: *Benefits of P5 Post-Processor*

Product	**Elapsed Time (NPP)**	**Elapsed Time (P5)**
PPC620-4X (logic)	61 hrs	10 hrs
Kodiak (SRAM)	67 hrs	5 hrs
1 Gb DRAM test site	144 hrs	18 hrs

Deposition of Refractory Absorber

Summary

A sputter deposition system for depositing the absorber, etch stop, and hardmask has been set up at the T. J. Watson Research Center inYorktown Heights and is now operational. The load lock, substrate transfer system, and sputter process control operate have proven reliable. Annealing is being done in batch mode in a furnace and single wafers are annealed in the stress measuring tool. Measurements show the film composition does not change with deposition conditions and deposition steady state is reached rapidly. The as-deposited stress can be controlled such that a final stress of 10-20 MPa is obtained following annealing by changing the sputtering pressure. The as-deposited stress shifts such that it is less compressive when changing from Si substrates to Cr-coated Si substrates to Cr-coated heavily-doped Si substrates

I. Sputtering System

An existing processing vacuum system, with a high vacuum cryopump, was modified so it could be used to sputter deposit both refractory x-ray absorber materials and the Cr etch-stop and hard-mask layers onto 100 mm diameter substrates. In order to maintain compatibility with Motorola, an existing MRC 5" x 15" magnetron sputtering source was used. In order to improve film uniformity, both thickness and stress, a planetary substrate platform was designed and built. Both the rotation speeds about the wafer center and about the center of the system are independently controlled. The system incorporates both process pressure and gas flow control. Two process gases, argon and nitrogen, can be used, although to date only non-reactive sputtering with argon has been done. To increase the system throughput and to eliminate the variations in the sputtering conditions that result from air exposure a load lock and transfer mechanism has been installed.

The planetary substrate holder has a three wafer capacity. After an initial learning curve it has operated without failure. Cr films for etch stop and hard-mask and Ta-Si films are being deposited. Downstream automatic pressure control is used with fixed, but adjustable, Ar gas flow rates. The pressure control is accurate to within 0.02 mTorr. Sputtering pressures in the range of 10 to 30 mTorr are used. Ar gas flow rates typically are 30 sccm and are accurate to better than 1 sccm. DC sputtering power control is used. The repeatability of the sputtering current and voltage is better then 0.5% with this control. Ta-Si resistivity sheet resistance repeatability is better then 1%. A Ta_5Si_3 sputtering cathode is being used. This results in a film composition of about $Ta_{73}Si_{27}$ as measured by Rutherford BackScattering (RBS). Film composition in not a sensitive function of deposition conditions.

For the Cr films, film thickness was measured with a profilometer by patterning the film with photoresist followed by etching with a Cr photomask etchant. The Ta-Si film thickness was also initially measured with a profilometer where the film was patterned using a silicon mask

during deposition. After the relationship between sheet resistance and thickness was determined, 4.09 ohms/square corresponding to 523.5 nm, the thickness was calculated using the sheet resistance. This method could not be used with the heavily doped silicon wafers used for making membranes due to the high electrical conductivity of this doped layer. When these samples were being coated, periodically an undoped wafer was loaded and coated for a thickness measurement.

II. Stress Measurement and Annealing

The stress in the deposited films is measured with a Tencor Flexus instrument. We first focused first on understanding how the Flexus stress measurement tool operates and how to calibrate it. The repeatability of measurements at room temperature and at 400 °C was determined. The standard deviation of multi-measurements is now 1.2 MPa for a 0.5 μm film deposited on a 620 μm thick silicon substrate, as shown in Figure 1. This standard deviation can be decreased by an order of magnitude by using 200 μm thick substrates.

This instrument measures the stress as a function of position on a line going through the center of the wafer. Measurements are repeated several times and averaged; this is necessary to obtain the above accuracy. We typically measure the stress along two orthogonal lines going through the center of the wafer. Average values for each direction are recorded. In addition to measuring the stress at room temperature, this instrument can also measure the stress as a function of temperature. This has been used sparingly because, for annealing temperature of 300°C, a measurement cycle, heating and cooling to near room temperature requires about 90 minutes. In this instrument, a He gas ambient is used. Most of the annealing work has been done in a furnace using an Ar ambient. These furnace anneals are usually done in batch mode, i.e., several samples are annealed at the same time. Room temperature stress measurements are made following the anneal. During anneals, the sample is held at the anneal temperature for 10 minutes. This anneal time was not varied. Motorola has determined that anneal times of about 3 minutes are sufficient, and that further time at temperature hase only a small effect on stress.

The compressive stress always decreases with annealing in inert gas ambients. If the stress becomes tensile, the magnitude of the tensile stress increases with further annealing. If there is oxygen in the annealing ambient the stress becomes more compressive with annealing.

Figure 2 is a measurement of film stress as a function of temperature. (Note: this is for a Ta-Si film despite the label in the figure showing an ID of Ta4B6.) The substrate is heated at a constant rate, held at 325°C for 10 minutes and then cooled to about room temperature. The final stress after annealing is 8.5 MPa. The slope of this curve is a measure of the differential thermal expansion coefficient. Figure 3 shows the stress measured at 325°C as a function of time; there is an interval of 40 seconds between each measurement as the substrate is held at temperature for 10 minutes. The figure shows a typical result for this material system: after about 2.5 minutes (record number 59 on the figure), the stress reaches its final value. Following the anneal shown in this figure, the final room temperate stress is -8.5 MPa. (Note also that in this figure the standard deviation indicated by Sigma is meaningless.)

III. Ta-Si Film Composition

After initial target problems, we have now been able to obtain films with good composition. The film composition, as measured by RBS, is, in atomic percent, $Ta_{73}Si_{27}$. Figure 4 shows a typical RBS spectrum along with a fitted spectrum. A carbon substrate has been used to reduce substrate interference. In this figure the intensity is on a log scale, and the fitted curve does not have the background added to it. One can see Ar in the film; there is about 0.5 ± 0.5 % Ar in the film. There is also a surface peak of Oxygen in this 330 nm thick film containing 1.5 x 10^{16} atoms/cm^2 in a depth of about 4.0 nm. These results are confirmed both by Auger and PIXE, Proton Induced X-ray Excitation, measurements. Unsuccessful attempts were made to measure variations in Argon content with deposition conditions. To do this the RBS dose was increased from the standard 10 μCoulombs to 50 μCoulombs. Even with this greater sensitivity, the variation in Ar concentration was less then our sensitivity. In sputtering from cathodes containing materials with significantly different masses, one often observes changes in film composition with time when deposition conditions are varied. This variation stops once steady state is reached. To characterize this effect with a Ta_5Si_3 cathode, films were deposited at 5 minute intervals, about 200 nm thick, following a change in sputtering pressure. The measurements show that this effect is not significant in the Ta-Si material system, i.e. no variation in film composition was observed. This shows that following a change in deposition conditions, a long presputtering time in not required.

IV. Cr Film Stress

Relatively little time was spent on controlling the stress in the 20 nm Cr etch stop layer deposited onto the substrate. The Ta-Si layer is deposited on top of this layer. Cr film stress was often 300-500 MPa. In order to increase the sensitivity of the stress measurement for the thin Cr films, very thin (0.18 mm thick) Si wafers were used. When Cr deposition conditions were varied, the stress measurements were inconsistent, probable due to the curvature of these very thin wafers. This work needs to be explored further.

V. Ta-Si Film Stress

The stress of the as-deposited Ta-Si films can be controlled with the deposition conditions. For a fixed sputtering power and Ar gas flow rate the stress varies systematically with the sputtering pressure, becoming less compressive with increasing pressure. However, the stress also varies with the substrate. Si wafers and heavily-doped Si wafers give different though consistent results. The roughness of these two types of wafers was measured using an atomic force microscope (AFM). The background surface roughness (rms) of all the observed boron-doped wafers was found to be around 2 nm for image dimensions ranging from 1 to 20 μm. However, the surfaces are covered with pits and trenches as deep as 40 nm. Wafer to wafer variation or spatial non-uniformity in this defect density could be at the origin of some stress variation. The defect density observed is in the range of 10^7 cm^{-2}. Further AFM measurements will be performed after deposition to determine if the roughness propagates

through the absorber layer. By comparison, the undoped Si wafers have an average roughness of only about 0.4 nm. We plan on systematically looking at the roughness dependence of the stress. The stress was also found to vary in a consistent way with and without a Cr layer on the Si.

Figure 5 shows the room temperature stress as a function of anneal temperature for 500 nm thick Ta-Si films deposited on undoped Si wafers. For all depositions 1.5 kW was used as the DC sputtering power; power control was used. The four groups of results are for different sputtering pressures, 22.5, 20.0, 17.5. and 15.0 mTorr. Our intent was to deposit films that would have a final room temperature stress of 1-2 MPa after annealing at about 300°C. The anneal temperature would then be used to control the value of the final stress value. From these results, 17.5 mTorr is the desired sputtering pressure. The as-deposited stress for this sputtering pressure is about -250 MPa.

When Ta-Si is deposited onto wafers that have a thin (20 nm) Cr film, the as-deposited stress of the Ta-Si film shifts. The stress becomes less compressive by about 250 MPa. Figure 6 shows the room temperature stress versus anneal temperature. Where the as-deposited stress was expected to be -250 MPa, these films were found to have a stress of -10 to 50 MPa. Figure 7 shows similar results for three wafers that were coated during the same deposition run at a sputtering pressure of 17.5 mTorr; two of the substrates had a Cr film while the third did not. Here the two orthogonal stress measurements for each wafer are shown. Figure 8 shows more results as a function of deposition pressure, also showing the effect of the Cr coating on the substrate. We see that for films deposited on Cr to be annealed to a final stress of 10-20 MPa, the sputtering pressure needs to be between 16.5 and 17.5 mTorr.

When heavily-doped B wafers (for making membranes) are used for substrates, the stress of the as deposited film again shifts so it becomes less compressive. All of these B-doped wafers had a 200 nm Cr film deposited prior to the Ta-Si deposition. Figure 9 shows some of these results. With a sputtering pressure of 15.5 mTorr the as-deposited stress is about 10 Mpa. To obtain the desired stress after annealing, the sputtering pressure needs to be reduced to 15.2 mTorr. This figure also shows the-as deposited stress of a substrate without the heavy B doping, coated along with some of the above B doped wafers, is -160 mTorr.

VI. Alternative Absorber Materials

We have also begun an investigation into alternative absorber materials to the TaSi which has been the focus of most of our efforts. An important criterion in selecting the elements forming the alloy is to constitute a compound that will absorb similarly to or more than the actual TaSi absorber. Starting from a lists of the energy dependent x-ray scattering factors, densities and atomic masses, we determined the transmission of a 0.5 μm thick layer of solid element as a function of x-ray energy from 10 eV to 30 keV. Comparison figures were made for the energy range of 0.9 eV to 1.7 keV in order to see the position of absorption edges in the energy range of interest for the x-ray lithography. To sort the elements in decreasing order of transmission, we integrated the transmission from 1 keV (1.2 nm) to 1.6 keV (0.8 nm) to get an average. Eventually, these averages need to be determined after the transmission has been weighted with

the synchrotron intensity versus energy curve. Table 2 shows a sorted list of the average transmission of the elements, assuming that the x-ray intensity is independent of the x-ray energy (flat spectrum); Figure 10 shows the transmission as a function of atomic number. As can be seen, many elements other than tantalum have larger absorption characteristics. For example, an element such as cobalt, which is three times lighter, absorbs about 30% more than tantalum (for same volume). We recently have modified our analysis program to calculate the transmission for a given alloy composition. For a first approximation, the density was considered linear with the volume percentage of each of the constituents. As the density of alloys is not always predictable, the program was also modified to accept an arbitrary (or measured) value for the density.

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Table 2

AVERAGE TRANSMISSION through 0.5 μm of element for the energy range 1 to 1.6 keV. (assuming x-ray intensity is independent of E)

U	0.02212	Tc	0.195	Y	0.6329
Pa	0.03528	Sn	0.1962	Sc	0.6556
Pt	0.05693	Gd	0.1996	Br	0.7563
Ir	0.05843	Sb	0.2075	Sr	0.7764
Os	0.0671	In	0.2107	Ne	0.778
Au	0.06888	Mn	0.2141	Kr	0.8065
Cu	0.07355	Te	0.2196	Mg	0.8105
Ni	0.08411	Tb	0.2269	Ca	0.8151
Th	0.08501	Dy	0.2442	Na	0.8191
Re	0.08679	Eu	0.2468	F	0.8426
Ce	0.1061	Hf	0.2485	O	0.8686
Co	0.1114	Cr	0.2517	Rb	0.8695
W	0.1146	Mo	0.2525	S	0.8696
Pm	0.1184	Ga	0.2601	C	0.8782
Zn	0.1201	Ho	0.2685	Ar	0.8818
Nd	0.1204	I	0.2714	Cl	0.8877
Ac	0.1213	Er	0.2898	Al	0.8938
Pd	0.1215	Tm	0.3116	K	0.906
Pr	0.1272	Nb	0.3349	**Si**	**0.9067**
Hg	0.1279	Ra	0.3421	P	0.9086
Rh	0.1308	Ba	0.3549	B	0.9294
Ag	0.1374	V	0.3571	N	0.9315
Sm	0.1406	Lu	0.3666	Be	0.9724
Ru	0.1507	Xe	0.3678	Li	0.9971
Tl	0.1522	Ge	0.368	He	0.9998
Pb	0.1557	Rn	0.4171	H	1
Fe	0.1616	As	0.4388	At	Density not available
La	0.1624	Yb	0.4554	Fr	Density not available
Ta	**0.1652**	Zr	0.4658		
Cd	0.1793	Ti	0.495		
Po	0.1819	Cs	0.5803		
Bi	0.1833	Se	0.5839		

TaSi X-Ray Mask Etching

I. Summary

Yorktown personnel provided consultation and guidance to the AMF concerning etching of the refractory absorber and hard mask, as well as resist strip issues.

The principle etching problem was that the recipe developed at Motorola for etching TaSi was not working properly in the AMF etch tool, e.g., there were issues with etching not starting, severe undercutting, and roughness at the interface between the TaSi absorber and the Cr etch stop layer. As a result of this effort, one etch process has been developed to give a nearly 90 degree profile of the TaSi absorber, with much less Cr roughness, and with a higher etch rate (the higher etch rate may not be desirable).

II. The Problems:

Initial results obtained during March showed that:

1) The etch of the TaSi layer did not start reliably at the DC bias from Motorola's recipe, i.e., 50 W (~ -145 V) with 20 sccm of Cl_2 and 2 sccm of O_2 at 2 mTorr of pressure.

2) By decreasing O_2 flow rates from 2 sccm to 1 or 0 sccm, and increasing RF bias power from 50 to 90 and 135 W, TaSi was etched but all showed severe undercut, i.e., negative profile.

3) Using one step etching with 25-35% of overetch process at different recipe conditions (e.g., different DC bias or O_2 flow rates), severe roughness, or a "grass-like" structure, appeared at the interface between the TaSi absorber and Cr etch-stop layer.

III. The Achievements:

No-Start-Etch

To address the problem of no-start-etch of TaSi, a longer cleaning and seasoning of the chamber were performed. The AMF has an almost identical etch tool to the one at Motorola, but Motorola uses the tool for three different etch processes, even though all three are chlorine-based chemistry. Motorola does routinely clean the chamber between each process. After the AMF tool was opened for replacing an O-ring, the chamber was cleaned by running more than 30 minutes of Ar/Cl_2 plasmas followed by a chamber seasoning procedure (Cl_2/O_2 plasma). After the chamber cleaning, we observed that the etch results still shifted with time, e.g., the RF bias requirements for start-etching of TaSi reduced as more TaSi parts were etched. A breakthrough

step with 20 sccm of chlorine only was added to the process to breakthrough the possible native oxide layer on the top of TaSi. The breakthrough step takes about 5-10 seconds dependent on RF bias; a bias of > 100 V provided reasonable results. Using the breakthrough step, a stable process was achieved for etching TaSi at 50 W of RF bias power.

Conclusion: Since the chamber wall effect is a very strong factor on the etch results, it is important to clean and season the chamber for a relatively long time after the chamber is exposed to air.

Further studies were conducted to assess the effects of chamber cleaning and conditioning. Appropriate conditioning procedures (O_2 plasma clean, followed by Cl_2 plasma etching of Si and TaSi substrates) to season the reactor walls were devised. Following this methodology, stable etch performance (measured in terms of line width and side wall angle) after chamber wet cleans could be expected.

Negative Profile (Undercutting)

To attempt to get a vertical profile, the RF bias during the etch was increased from the 50 W of Motorola's recipe to 135 W. The DC bias was varied from 145 V to 220 V. The etch results showed that the combination of DC bias and O_2 flow rate (0 to 2 sccm in 20 sccm of chlorine) changed the profile angle from negative to positive. Very narrow structures, such as 0.1 μm lines, were lifted during etching using 135 W of bias, but no line was lifted using 50 or 100 W of bias power.

The Cl_2 flow rate was reduced to reduce undercutting of the TaSi profile. In the etching of TaSi using chlorine/oxygen chemistry, the profile angle was controlled by a sidewall passivation layer formed by the oxides of Si and Ta containing some carbon (from the sputtering of the photoresist mask) or chlorine. The thickness of the sidewall depends upon the concentrations of both oxygen and chlorine. Oxygen increases the thickness whereas chlorine reduces the thickness. In general, too high a concentration of oxygen tends to oxidize the bottom surface of the trench to reduce the etch rate, erodes the photoresist mask, and increases the roughness of narrower trenches. It also reduces the selectivity of TaSi over the Cr etch stop layer. On the other hand, if too many chlorine atoms arrive the bottom of the trench, some of them are consumed by etching the TaSi at the bottom of the trenches, while some of the unconsumed chlorine atoms bounce back to attack the sidewall to cause sidewall erosion or undercutting due to the thinner passivation layer on the deeper (or freshly etched) sidewall surfaces. This has often been seen with slower etching materials, such as an etch stop being exposed to the plasma. But too low a concentration of etchants, e.g., chlorine, may result in a more severe microloading effect. The conventional way to reduce etchant concentration is to add inert gases, such as He or Ar. A part etched in 10 sccm of chlorine showed a straighter profile.

Results: Because of limited availability of samples, the experiments were focused on tuning the DC bias. A part etched in 100 W (~ 145 V of DC bias) with 20 sccm of Cl_2 and 2 sccm of O_2 showed a satisfactory profile from 0.175/0.2 to 0.5/0.5 μm structures.

Interface Roughness

The first step taken to address the problem of interface roughness interface was to identify the causes of the roughness. After severe roughness appeared at the interface of the TaSi and Cr etch-stop layer, partially etched parts, i.e., etch stopped right at the OES endpoint, were used to check the origin of the roughness, which could be due to non-uniform breakthrough, to sputtering of the photoresist mask materials, to microloading (or so-called aspect ratio dependent etching, ARDE), to non-uniform Cr material, etc. A non-uniform Cr layer did not seem to be the sole reason for the roughness, since roughness was also observed on samples without a Cr layer, though it appeared much less severe. Aggressive chemical etching, e.g., using pure Cl_2 plasmas and physical sputtering using pure Ar plasma all reduced the roughness on the bottom the trenches.

To reduce the roughness and clear any remaining TaSi in the narrower trenches, an overetch step was also introduced using different chemistries, e.g., adding Ar and DC bias on parts with and without a Cr etch-stop layer. A few parts etched with or without an overetch step under different conditions showed significant improvement on the roughness of narrow trenches.

Further analysis indicated that there were differences between the Motorola and AMF etch systems that caused them to operate in different process regimes. Some engineering modifications had been made to the AMF electrode plate when it was first installed, and this became the focus of closer examination. Measurements of the electrode-sample gap in the Motorola and AMF systems indicated that the gap in the AMF system was 0.8 mm while the gap in the Motorola system was 0.4 mm. This difference is quite significant in terms of heat transfer from the sample to the electrode (the electrode-sample temperature difference in the AMF system was about twice as large as at Motorola). In addition, the larger gap reduced the RF capacitive coupling to the sample. The Motorola electrode plate was shipped to the AMF for testing. Once it was installed in the AMF system, the "grassy" residue was no longer present. The AMF electrode plate has been modified to match so the Motorola plate, which has been returned.

Resist Stripping

In the case of resist stripping, a variety of O_2/CF_4 plasma chemistries were evaluated to assess effectiveness of resist stripping after SiON etch (before TaSi etch). This change in process integration (previously the resist layer was left on in the TaSi etch) did not adversely affect etch performance, and may have improved nested-to-isolated etch bias. It was previously thought that resist was playing an important role in the TaSi etch, but this does not appear to be the case. Continued improvement of the nested-to-isolated bias, particularly for 150-130 nm features, is the focus of ongoing work. Smaller dimensions will be addressed as samples with sub-130 nm patterns become more readily available.

Evaluation of NTT Stress Measurement Tool

Description

An absorber with uniform stress or with small stress variations across the membrane is necessary to meet the image placement requirements of x-ray masks. Sputter deposition of refractory metals with uniform stress is a major technical challenge, particularly when the deposition is carried out on membranes. Even when the deposition is carried on wafers, obtaining uniform stress has required a major development effort. This effort has been hampered by the difficulty in reliably measuring stress uniformity on thick (500 - 600 μm) substrates.

NTT-AT has a stress measurement apparatus which is believed to be available for purchase. NTT-AT claims that the apparatus is capable of measuring local film stresses, with a good spatial resolution, when the films are deposited on substrates with a thickness on the order of 600 μm. The technique used relies on measuring the deflection (bow) of the substrate wafer, with and without the film of interest, using a laser reflection method. Local mapping of the bow is achieved by x-y movement of the substrate using an accurate stage. The stress is calculated from the local bow using Stoney's equation. The claimed accuracy and sensitivity of the apparatus is on the order of a 0.2 to 0.3 x 10^7 dynes/cm^2.

Given the stiffness of a 600 μm silicon wafer, the low magnitude of the film stresses of interest, and the technique used to determine stress, it is justified to question the ability of the apparatus to meet the claims. On the other hand, if the apparatus were to meet the claims, it would constitute a very valuable development tool for characterization of absorber stacks. The problem so far had been to devise a methodology for testing the apparatus, i.e., for providing samples with well-defined areas of known varying stress.

Four samples, prepared as described below, were sent to NTT-AT. The small number of samples was dictated by the high cost per sample charged to perform the measurements; promising results would justify a thorough evaluation using more samples.

Test Methodology

The four samples submitted, on 2-side polished Si wafers, approximately 500 μm thick, consisted of two PMMA and two gold films.

The PMMA films were spun from "standard" PMMA solution (490k mol. wt. in diglyme), spun and baked at 170°C. The thickness of these films was 700 nm, and the nominal (unexposed) stress was 1 x 10^8 dyne/cm^2. Based on work done last year, areas of different stress values were produced in these films by exposing selected areas to different doses of UV radiation from a mercury lamp. Both large and small areas of reduced stress were created to test the spatial resolution of the tool.

The gold films were obtained using the POR electrodeposited gold. In this case the different "effective stress" areas were achieved by producing areas of different thickness. Because the NTT apparatus uses Stoney's equation to calculate stress, areas of different thickness will appear as areas of different stress when the calculation assumes a film with uniform thickness. Both large and small areas of thicker gold were created to test spatial resolution.

Specifically, the four samples were:

1) A 4" silicon wafer coated with PMMA as described above. Large areas with stress of of 0.5, 0.2, and 0.1 times the nominal (shown as the vertical rectangles in the upper part of the wafer in Figure 11) were created through exposure. Smaller areas (1x1 to 3x3 mm^2) of reduced stress values were similarly created in the areas shown as squares in Figure 11.
2) Identical to Sample #1
3) A 4" silicon wafer coated with 330 nm of gold (having a stress of 1×10^8 dyne/cm^2), except in the patterned areas shown in Figure 12, where the gold thickness was 1030 nm (for a stress of approximately 3×10^8 dyne/cm^2).
4) Identical to Sample #3, except that the thicker gold was only 730 nm thick (for a stress of approximately 2×10^8 dyne/cm^2), as shown in Figure 13.

Results

The nominal stress values achieved for selected areas in samples were measured using the NTT apparatus. If one disregards the *absolute value* of the stress, the results for Sample #1 showed some qualitative agreement with what was expected, but *only* within a square area in the middle of the wafer. Outside of this area the stress distribution appeared to bear *no correlation at all* to the stress of the film supplied. The spatial resolution was also found to be poor: the large areas of different stress were bound by fairly sharp, straight, edges, but they appeared fairly diffuse in the stress map provided by the NTT tool.. Furthermore, the small patterned squares did not show up in the plot, not even the larger ones which measure 3x3 mm^2.

The stress maps produced by the NTT apparatus for Samples #2-4 again showed no relationship to the stress distribution in the samples submitted for measurement, even when one disregards the absolute value of the stress in question. In the case of Sample #4, there *may* have been some resemblance to the stress distribution indicated from the NTT tool if one assumes that the patterned area and the measurement area are displaced relative to each other in the vertical direction. Even with this allowance, one is hard put to justify a small area of high stress that appeared in the NTT map. Furthermore, the stress values indicated for Samples #3 and #4 relative to each other were the reverse of the relative stress values of the samples submitted; this gives one reason to suspect that the apparent resemblance may just be a fluke.

In summary, from the small number of samples measured it appears safe to conclude that the NTT apparatus *does not* have the stress mapping capability claimed. Further expense and effort in evaluating this apparatus is not considered justifiable.

Evaluation of Chemically Amplified Resists for X-Ray Mask Applications

In an effort to find an etch resistant photoresist for x-ray mask applications, several commercially available photoresists were evaluated. To date, three negative tone photoresists and one positive tone candidate have been examined. Evaluations on a second positive tone resist were started but discontinued due to poor resolution of the material, and work on a third positive tone material is in progress. Lithographic attributes such as resolution, sensitivity, dose latitude, thinning, and resist profile have been investigated. Particular attention has been paid to the post exposure bake latitude because of temperature uniformity issues related to baking on a membrane. Shelf life on a coated substrate is another important characteristic, since x-ray masks may be coated and stored in the e-beam chamber for at least 8 hours for temperature stabilization before exposure. Environmental stability after exposure and during long write times was also examined. All exposures were done on a 25 kV vector scan system with a 25 nm spot size. Proximity corrections previously determined to produce 50 nm isolated lines in one of the negative tone resists were used for all of the evaluations.

The three negative tone resist candidates were Shipley's SNR, IBM's CGR, and TOK's EN-002. SNR material was evaluated so that a direct comparison could be made between the process currently being practiced in Burlington and the results obtained here. Of these three materials, CGR has the best resolution, is the most sensitive, and has the best post exposure bake latitude. However, the shelf life on a coated substrate for CGR does not meet the minimum 8 hour requirement. There are plans to evaluate CGR with a conducting top coat to determine if the shelf life of the material can be extended. Table 3 summarizes the results from the negative tone candidates.

The positive tone materials under investigation are IBM/Shipley's UV3 and UV6, and TOK's EP-002. The UV3 work has been completed, the UV6 work is currently in progress, and the EP-002 evaluations have been suspended due to resolution problems with the material. The vendor is currently looking into the problem, and if a new sample or new processing conditions for the existing material are provided, then the evaluations will be completed. Table 4 summarizes the results from the positive tone materials.

Table 3. *Summary of negative tone candidates.*

Resist	EN-002	CGR	SNR
Thickness (μm)	0.38	0.31	0.38
Resolution (isolated lines, nm)	50 (not linear)	50 (not linear)	50 (not linear)
Resolution (equal lines/spaces, nm)	150	150	150
Resolution (isolated spaces, nm)	>500	250	>500
Profile	vertical, top slightly rounded	vertical, top slightly rounded	vertical, top slightly rounded
Sensitivity ($\mu C/cm^2$)	4.5	2.3 for 50nm gates, 2.8 for linear	7.25 for 50nm gates, ~8 for linear
PEB Latitude (nm/°C)	7	3.2	10.6
Linewidth vs Dose (%/%)	1.5	1.1	1
Thinning (nm)	30	40	30
Environmental Stability (out of tool)	>4 hrs, <24 hrs	>4 hrs, <24 hrs	<2.5 hours
Stability (writing time)	3 hrs	3 hrs	3 hrs
Shelf Life Coated	>8 days, <15 days	4 hours 50nm, 24 hours 250nm	>8 days, <14 days
Process	wafer	wafer	wafer
PAB (T-t)	100°C, 90 sec	95°C, 60 sec	115°C/120 sec
PEB (T-t)	130°C, 90 sec	95°C, 90 sec	105°C/120 sec
Developer	0.26N TMAH	0.14N TMAH	0.14N TMAH
Supply	TOK	IBM	Shipley
Solvent	PGMEA	PGMEA	PGMEA

Table 4. *Summary of positive tone resist candidates.*

Resist	**UV3**	**UV6**
Thickness (μm)	0.38	0.38
Resolution (isolated lines, nm)	150	250
Resolution (equal lines/spaces, nm)	150	
Resolution (isolated spaces, nm)	50/75	50
Profile	vertical	undercut
Sensitivity (μC/cm^2)	5	
PEB Latitude (nm/°C)	5.6	11.4
Linewidth vs Dose (%/%)	0.78	
Thinning (nm)	25	
Environmental Stability (out of tool)	>4 hrs, <24 hrs	
Stability (writing time)	3 hrs	
Shelf Life Coated	>5 days, <7 days	
Process	wafer	wafer
PAB (T-t)	140°C, 180 sec	140°C, 60 sec
PEB (T-t)	140°C, 120 sec	135°C, 90 sec
Developer	0.26N TMAH	0.26N TMAH
Supply	Shipley	Shipley
Solvent	Ethyl Lactate	Ethyl Lactate

Non-Chemically Amplified Resists for Mask-Making

Chemically amplified resists exhibit excellent resolution and sensitivity, however, they are extremely sensitive to environmental contaminants. In addition, they are very sensitive to temperature fluctuations during the post apply and post expose bake processes resulting in significant linewidth variation per degree temperature variation. For these reasons we have been focusing on developing a non chemically amplified resist for mask making applications. This activity has focused on evaluation of commercial resists and development of new resist systems.

ZEP 7000 is a commercial electron beam resist which is non chemically amplified. Although this resist has excellent resolution down to 0.1 um, it exhibits low contrast and does not have adequate etch resistance. We have been working on understanding what limits the contrast in this system and evaluating alternate developers to enhance the contrast. The developer recommended by the manufacturer is diethylketone/diethylmalonate 50/50. We have looked at a number of alternatives and find that one potential system is diethylketone/PGMEA 75/25. This work is on-going.

Parallel to this activity, we have been working on developing new non chemically amplified resists. Previously, we had found that polyhydroxyethylmethacrylates underwent efficient deesterification upon electron beam exposure resulting in the formation of methacrylic acid. This resist was positive tone, aqueous base developable and exhibited sensitivity on the order of 5 $\mu C/cm^2$. Although this resist exhibited lithography similar to chemically amplified resists, it did not have etch resistance. Therefore, we have been focusing on incorporating etch resistance into this type of polyhydroxymethacryate polymer by copolymerization with monomers containing etch resistant functionality. Some of these include methacrylate monomers containing cycloaliphatic groups such as isobornyl and aromatic groups such as styrenes, benzyl, and so on. It has been found that many of these copolymers exhibit excellent etch resistance, however, as a result of incorporating etch resistant groups, some deterioration of the lithographic properties in particular a decrease in sensitivity of the resist was observed. Currently, we are focusing on manipulating the chemistry of these resists either by copolymerization or blending with other polymers to result in a resist that may possibly combine good lithography with good etch properties.

Measurement of Resist Stress and of Stress Changes Caused byExposure

The stress and stress changes after exposure were measured for SNR and UVIII resists. The methods used were resonant frequency (RF) and out-of-plane distortion (OPD). For both resists it was found that the stress after post-apply bake was smaller than the detection limit of the RF method (approximately 10^7 dyne/cm^2 for the composite resist/membrane). Likewise, the stress change was smaller that the resolution limit of both RF and OPD methods. Consequently, change in stress during writing is not believed to be a significant contributor to placement accuracy when using either of these resists.

Sub-0.13 μm Mask Patterning

To evaluate CD control while printing patterns with dimensions of less than 0.2 μm, a gold plated x-ray mask with a minimum feature size of about 75 nm has been patterned using the VS-5 e-beam machine in Yorktown Heights. This LTM-4 mask contains extensive arrays of proximity effect corrected linewidth test patterns for both Prometrix and SEM measurements. The mask was returned to the AMF for final processing and metrology and has subsequently been delivered to ALF where it is being used in printing extendibility studies.

Additional characterization of the VS-5 tool has also been performed. Large x-ray masks are exposed in the system by accurately stitching a large number of exposure fields. This requires a very accurate table, which in practice is achieved by applying a set of correction factors to the "dead-reckoning" position. A matrix of marks has been exposed in VS-5 and measured in a Nikon 3i laser interferometric metrology system. This procedure provides an accurate and up-to-date determination of the correction factors.

Further work has also been done on advanced post-processing for x-ray mask data preparation. Monte Carlo simulations were performed for exposures on refractory mask substrates, including effects due to fast secondary electrons. The results were used as the basis for proximity correction parameters. Parameters were determined for both a 2-Gaussian and a multiple-Gaussian correction and transferred to the AMF.

In addition, the Dose6 version of proximity correction was investigated. The Dose6 algorithm was compared to earlier versions (Dose5X, Dose5XE, and Dose3) for a dose matrix test pattern. The Dose6 results (using PowerProx written in the C programming language) were found to be comparable to the earlier NPP versions implemented in FORTRAN.

Late in the year, VS-5 developed a vacuum leak and a problem with the 100 kV high voltage power supply. The vacuum leak was tracked to a leak in the gun ceramic. The original vendor of the gun, FEI Company, Hillsboro, OR, neither had the resources (no high voltage test stand) nor any prior experience repairing leaks in 100 kV gun ceramics. After a series of tests the vacuum leak was successfully repaired at IBM.

The high voltage power supply failed most likely as a result of a lightning induced brown-out in combination with a high current limit condition (> 150 microamps) resulting from a deteriorating plastic socket adapter in the gun. The socket appears to shows a temperature dependent leakage current that will lead to a high current limit condition if the atmosphere side of the gun high voltage feedthrough is merely purged with SF_6. The heat transferred from the thermal field emitter to the SF_6 gas and the socket raises the conductivity of the socket. As a measure to stabilize the situation, dry, cool nitrogen has been bled into the atmosphere side of the gun high voltage feedthrough. As a result the high voltage leakage current was reduced to less than 2 microamps, which is very close to the high voltage cable leakage current. With this temporary repair VS-5 is back in operation at 50 kV and initial test pattern exposures show 100 nm minimum feature size. A higher voltage operation will require further debug and testing to

evaluate the higher possibility of arcs while operating with dry nitrogen rather than SF_6 and finding a more permanent solution for the leakage current problem with the present plastic socket.

Investigation into the Cause of Accidental Mask-Wafer Contact during Stepper Handling

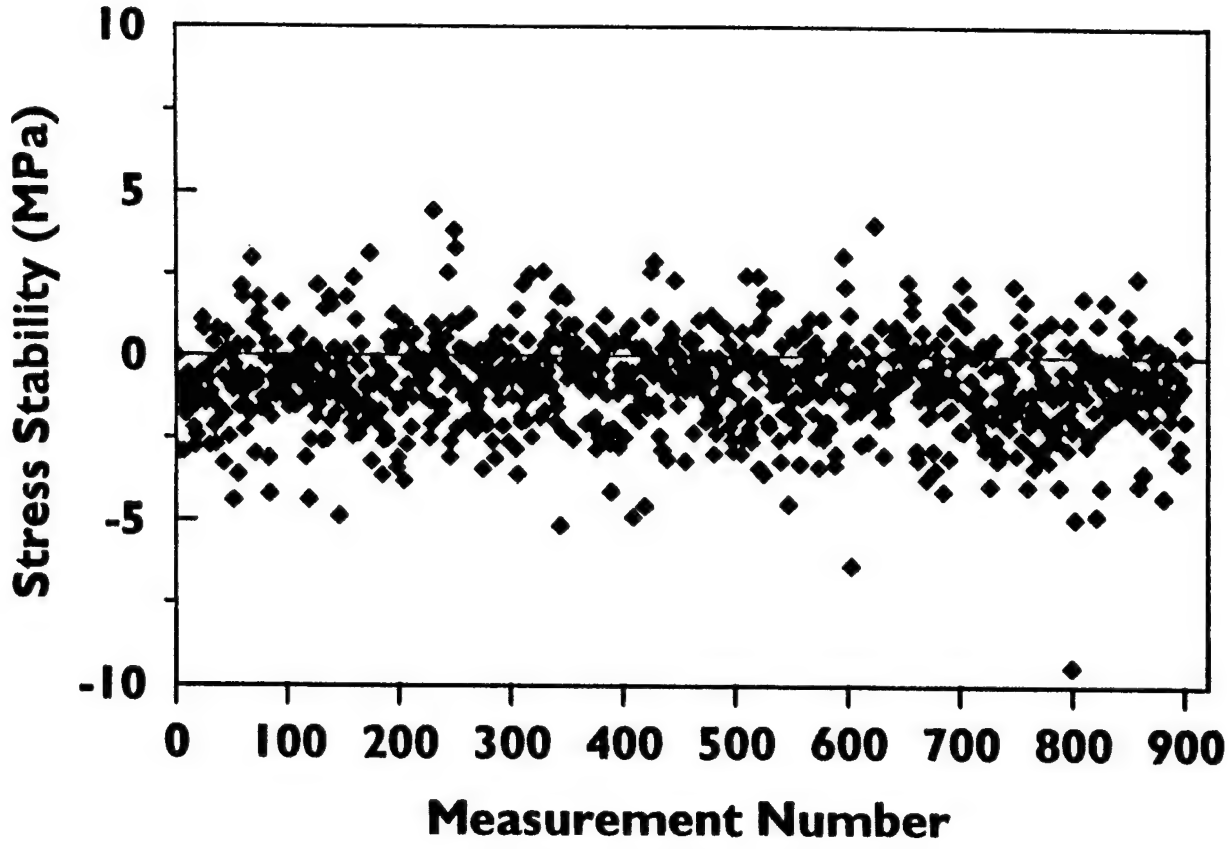
The stress of the gold absorber and overall flatness of several Phoenix masks were measured in an attempt to find the cause of unwanted contact of the masks with the wafers during exposure. The gold stress was found to be within specifications and was deemed not to be the problem. On the other hand, it was found that even though the mask flatness was within specs for all masks, in some cases the mask topography was far from the desired dome shape: some masks show bumps and ridges in the vicinity of the exposure area, which could act as barriers for the helium flow and hence lead to unpredictable membrane deformations when the mask is moving relative to the wafer. It was recommended that the flatness specifications be modified to take into account shape as well as overall flatness. Appropriate mask shape is also important for operation at small mask to wafer gaps.

Program Management Support

Program management support has been provided during this period, including:

- Program Management for the Proximity X-Ray Lithography Association
- Management of contract activities in Yorktown Heights, including generation of progress reports
- Attendance at conferences in the U.S., Japan, and Korea to represent our x-ray lithography program, and exploration of possible joint activities in x-ray lithography with other organizations in Japan and Korea
- Representation of X-Ray Lithography as Technical Champion in presentations to the SIA Lithography TWG and at Sematech workshops
- Preparation of a White Paper on X-Ray Lithography for use at the Sematech Next Generation Lithography Workshop to be held in November
- Meetings with representatives of DARPA and other government agencies concerning technical progress, contracts, and funding for x-ray lithography
- Meetings and discussions with Sematech management concerning x-ray lithography and possible Sematech support for x-ray activities, which has led to Sematech funding for certain activities in ALF
- Organization of and presentations at the MMD Executive Review/SIA TWG X-Ray Lithography Critical Review held in East Fishkill on 22 October, 1997

Stress Measurement Stability



- Stability measurement for phantom film of 0.5 um
- Standard deviation of measurement: 1.2 Mpa.

Figure 1

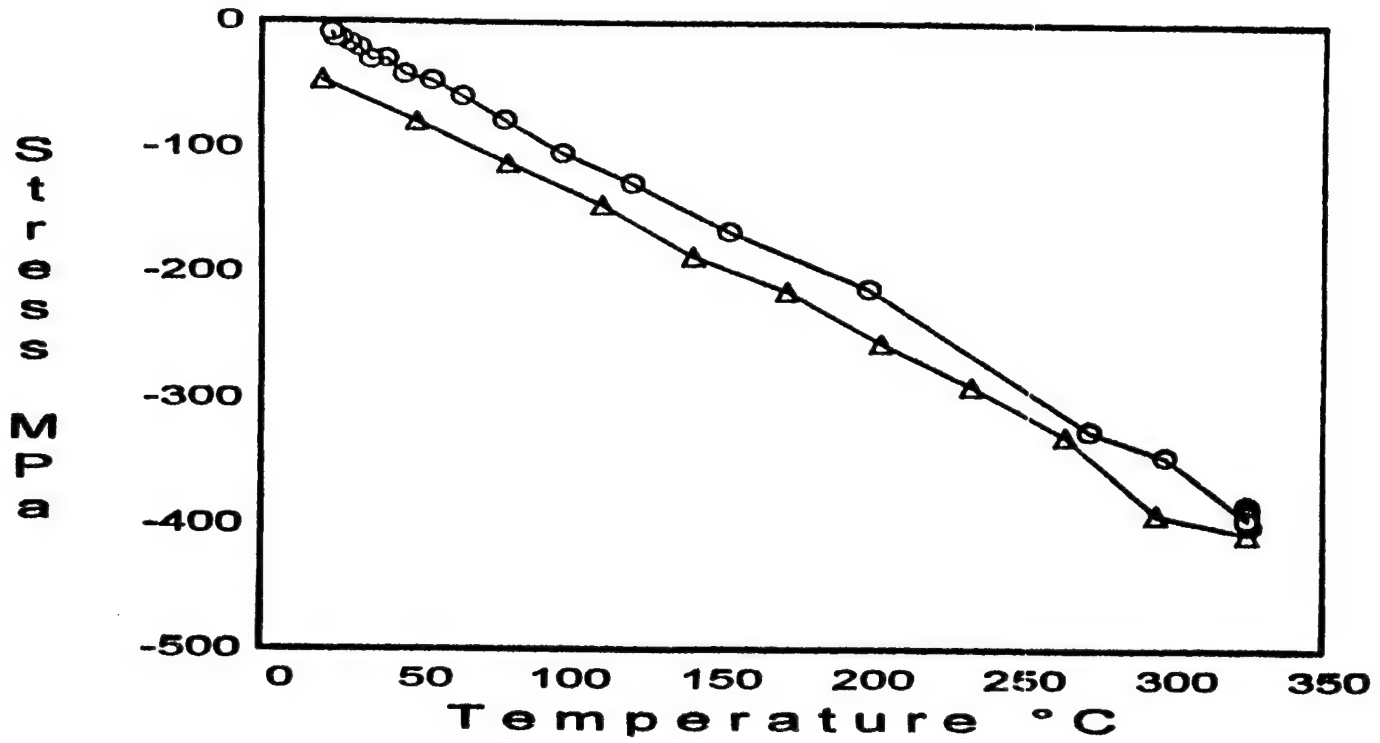

0
-100
-200
-300
-400
-500
Stress MPa
0
50
100
150
200
250
300
350
Temperature °C

Figure 2

Stress at 325C; final stress 8.5MPa; 10 min. measurement

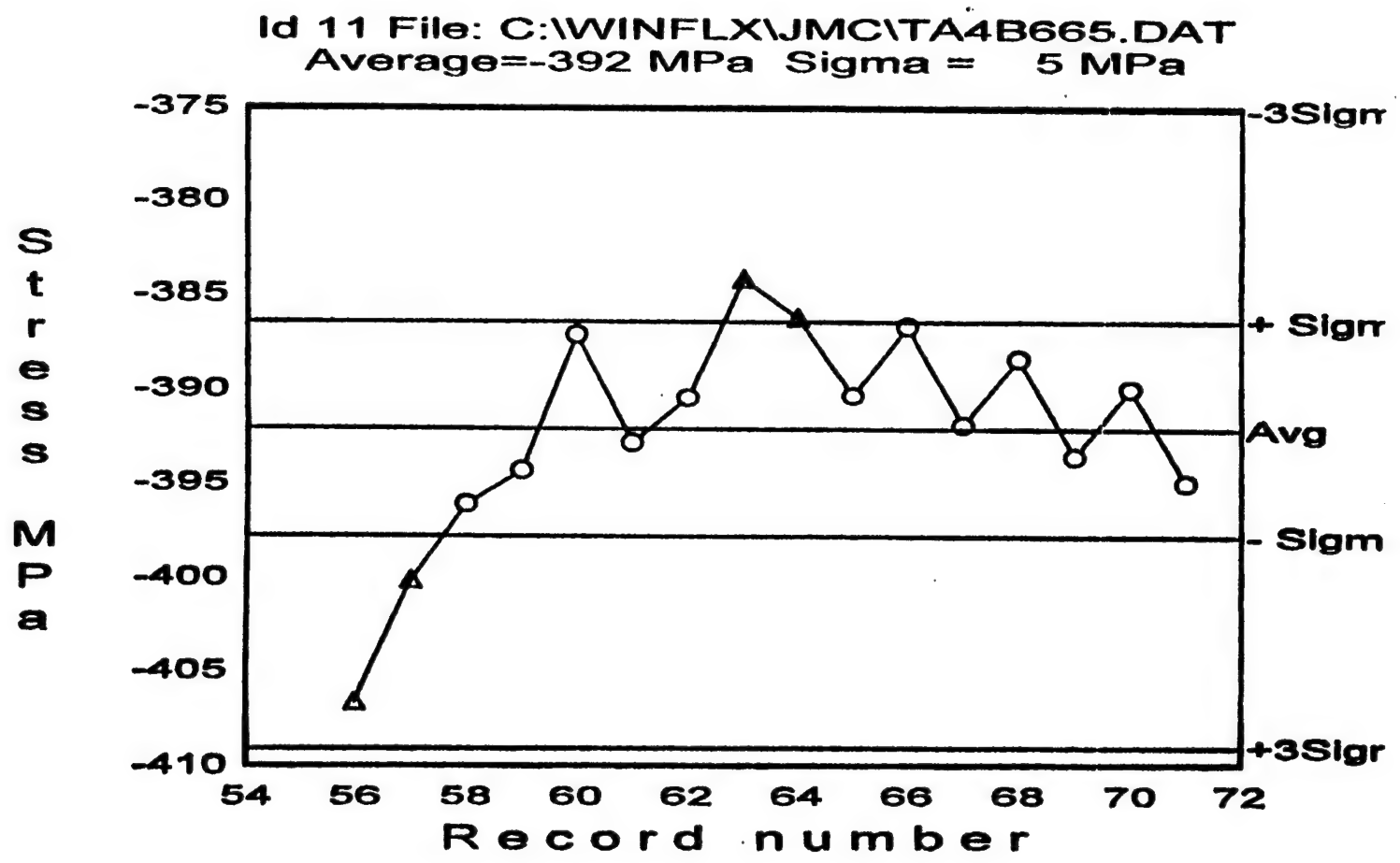


Figure 3

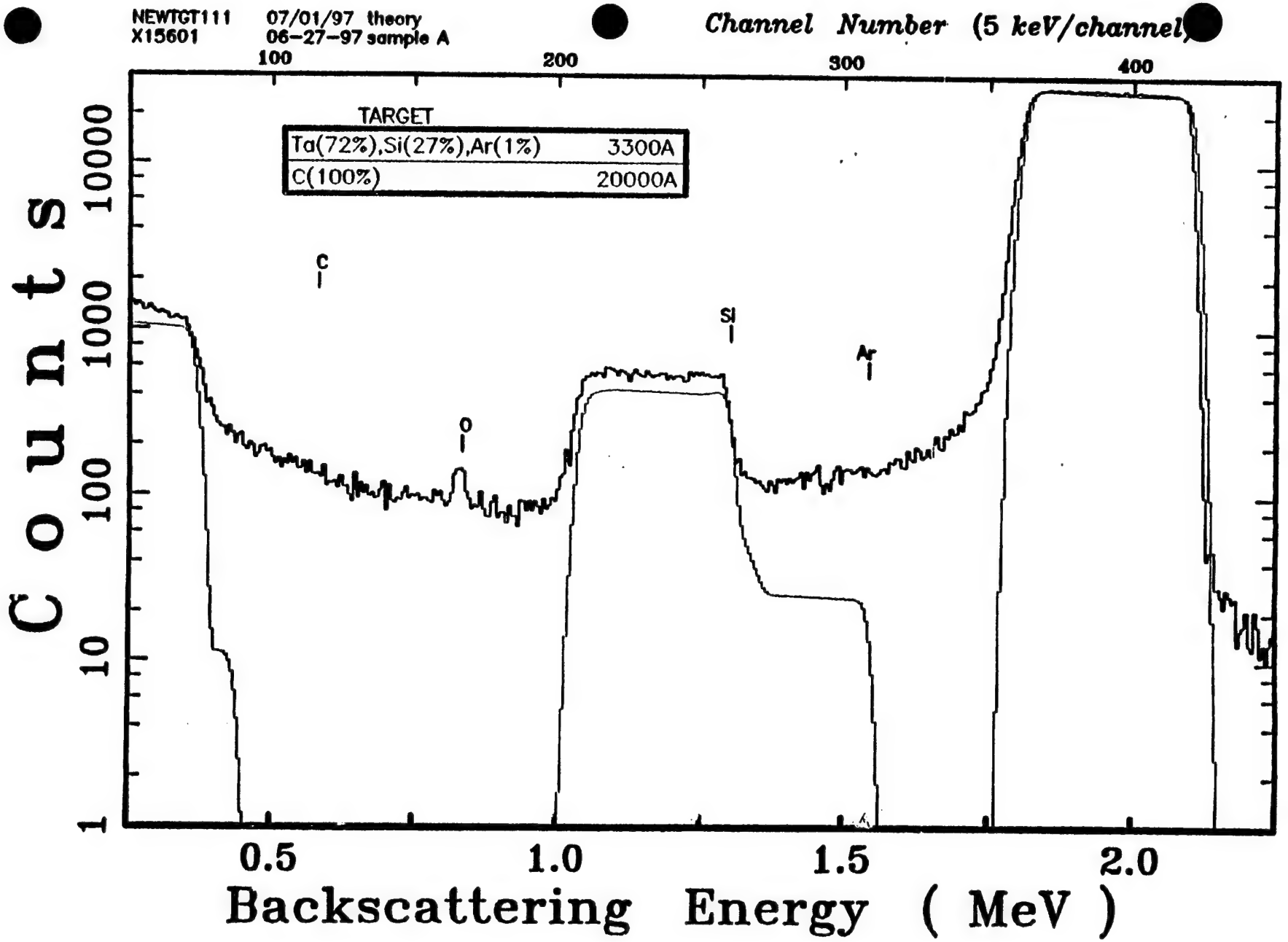

NEWTGT111 07/01/97 theory
X15601 06-27-97 sample A
Channel Number (5 keV/channel)
100
200
300
400
TARGET
Ta(72%),Si(27%),Ar(1%) 3300A
C(100%) 20000A
C
O
Si
Ar
Counts
10000
1000
100
10
1
0.5
1.0
1.5
2.0
Backscattering Energy (MeV)

Figure 4

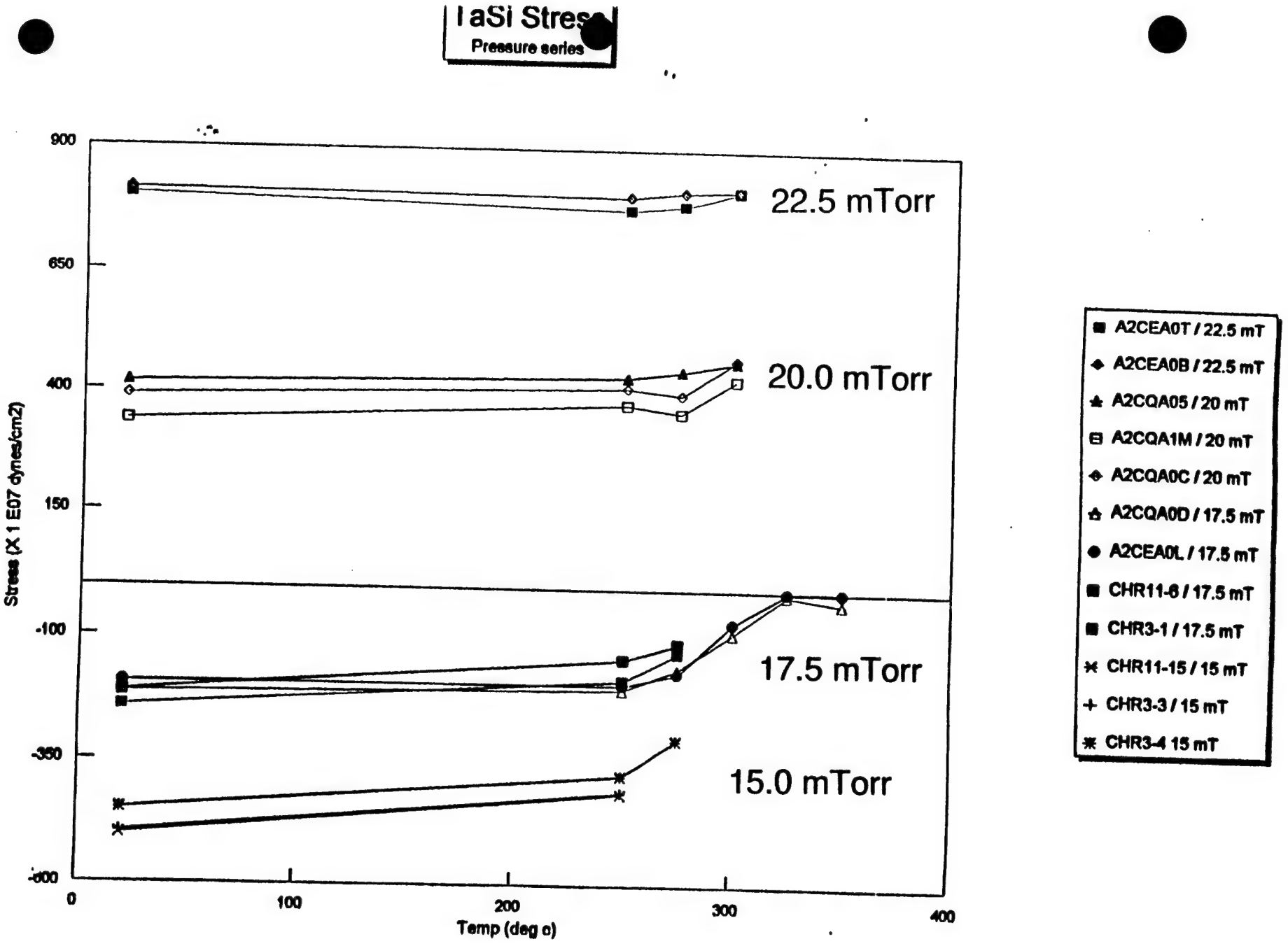

TaSi Stress
Pressure series
900
650
400
150
-100
-350
-600
0
100
200
300
400
Stress (X 1 E07 dynes/cm2)
Temp (deg c)
22.5 mTorr
20.0 mTorr
17.5 mTorr
15.0 mTorr
A2CEA0T / 22.5 mT
A2CEA0B / 22.5 mT
A2CQA05 / 20 mT
A2CQA1M / 20 mT
A2CQA0C / 20 mT
A2CQA0D / 17.5 mT
A2CEA0L / 17.5 mT
CHR11-6 / 17.5 mT
CHR3-1 / 17.5 mT
CHR11-15 / 15 mT
CHR3-3 / 15 mT
CHR3-4 15 mT

Figure 5

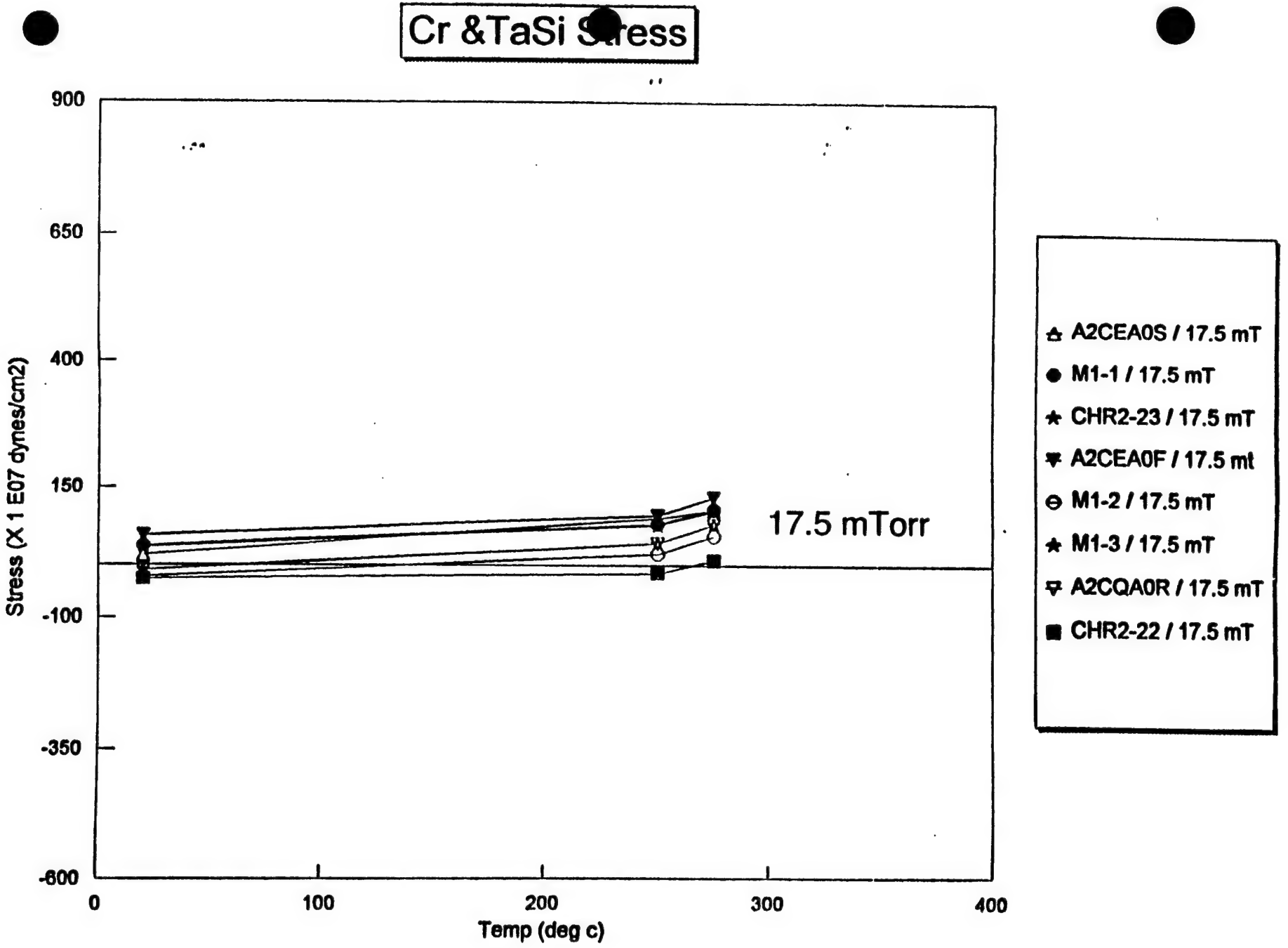

Cr &TaSi Stress
900
650
400
150
-100
-350
-600
Stress (X 1 E07 dynes/cm2)
0
100
200
300
400
Temp (deg c)
17.5 mTorr
A2CEA0S / 17.5 mT
M1-1 / 17.5 mT
CHR2-23 / 17.5 mT
A2CEA0F / 17.5 mt
M1-2 / 17.5 mT
M1-3 / 17.5 mT
A2CQA0R / 17.5 mT
CHR2-22 / 17.5 mT

Figure 6

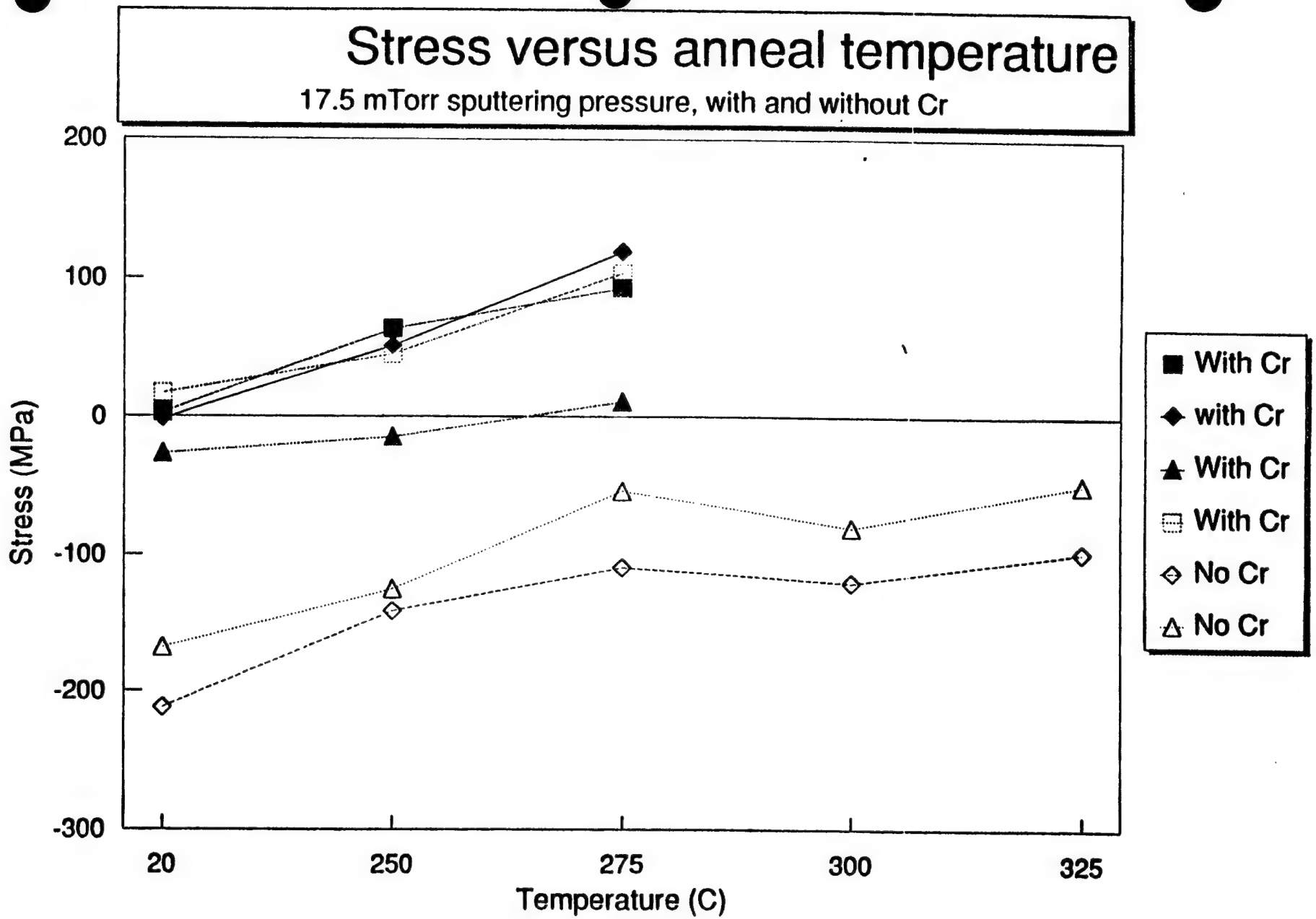

Stress versus anneal temperature
17.5 mTorr sputtering pressure, with and without Cr
200
100
0
-100
-200
-300
Stress (MPa)
20
250
275
300
325
Temperature (C)
With Cr
with Cr
With Cr
With Cr
No Cr
No Cr

Figure 7

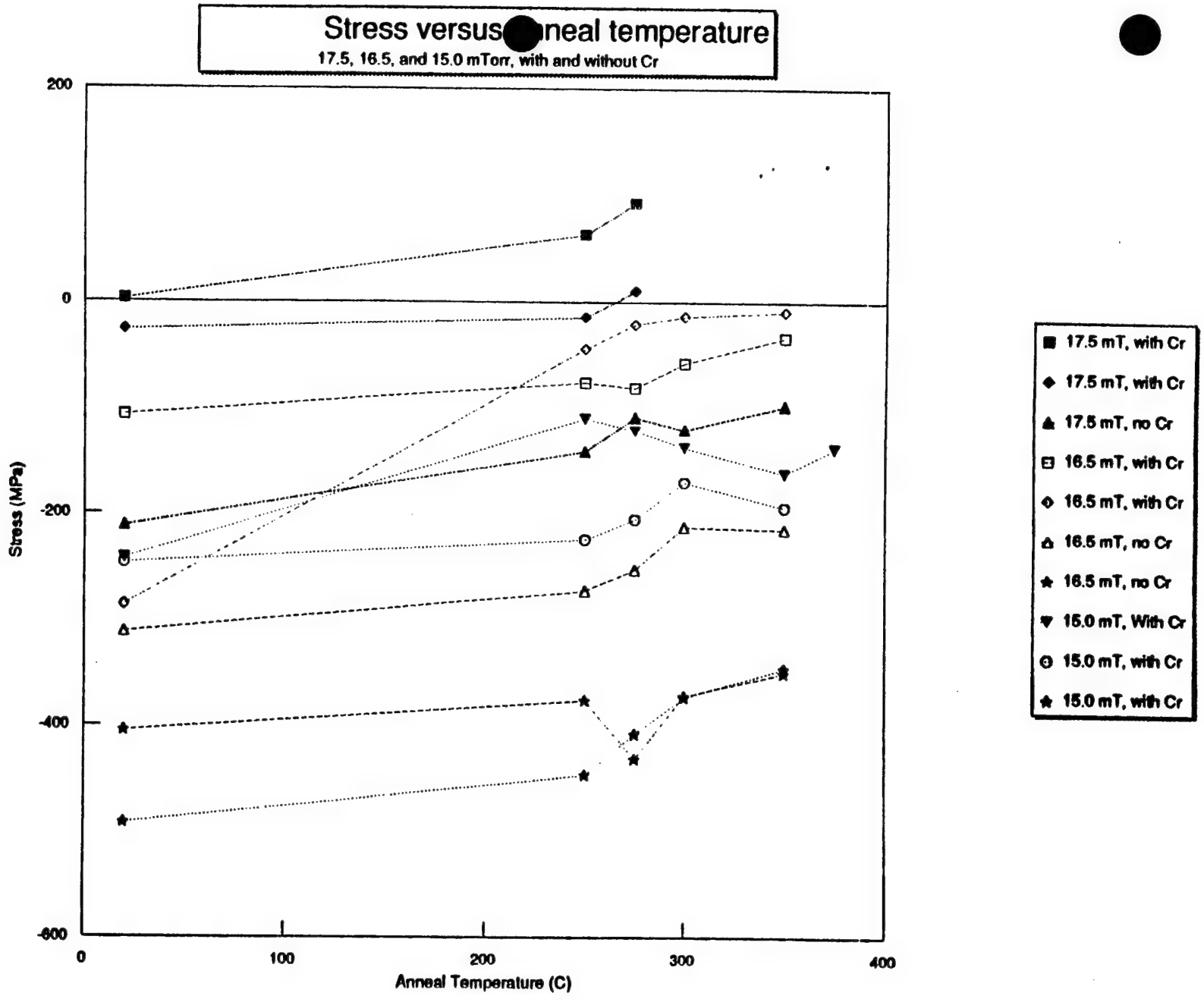

Stress versus Anneal temperature
17.5, 16.5, and 15.0 mTorr, with and without Cr
Stress (MPa)
200
0
-200
-400
-600
0
100
200
300
400
Anneal Temperature (C)
17.5 mT, with Cr
17.5 mT, with Cr
17.5 mT, no Cr
16.5 mT, with Cr
16.5 mT, with Cr
16.5 mT, no Cr
16.5 mT, no Cr
15.0 mT, With Cr
15.0 mT, with Cr
15.0 mT, with Cr

Figure 8

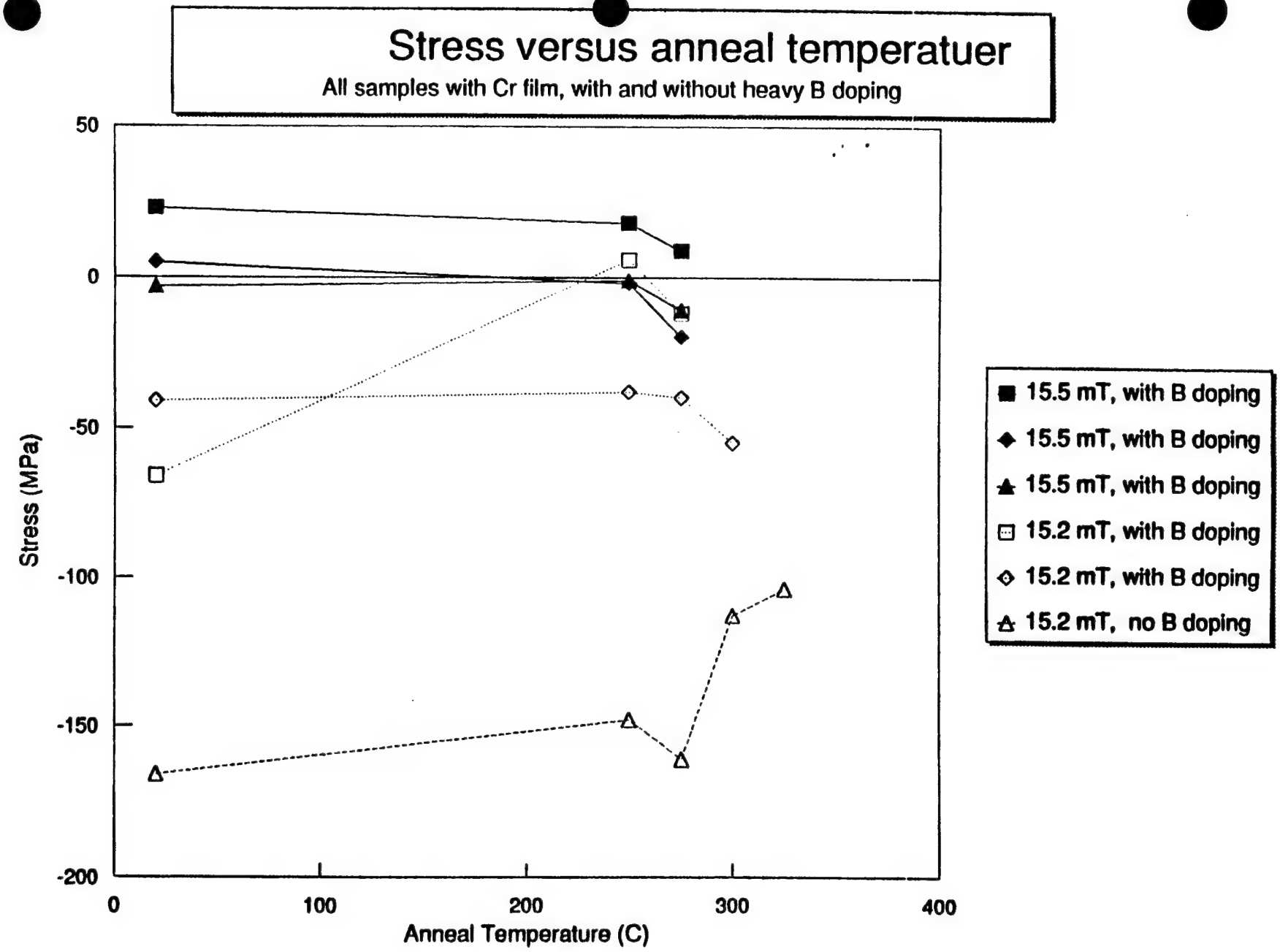

Stress versus anneal temperatuer
All samples with Cr film, with and without heavy B doping
50
0
-50
-100
-150
-200
Stress (MPa)
0
100
200
300
400
Anneal Temperature (C)
15.5 mT, with B doping
15.5 mT, with B doping
15.5 mT, with B doping
15.2 mT, with B doping
15.2 mT, with B doping
15.2 mT, no B doping

Figure 9

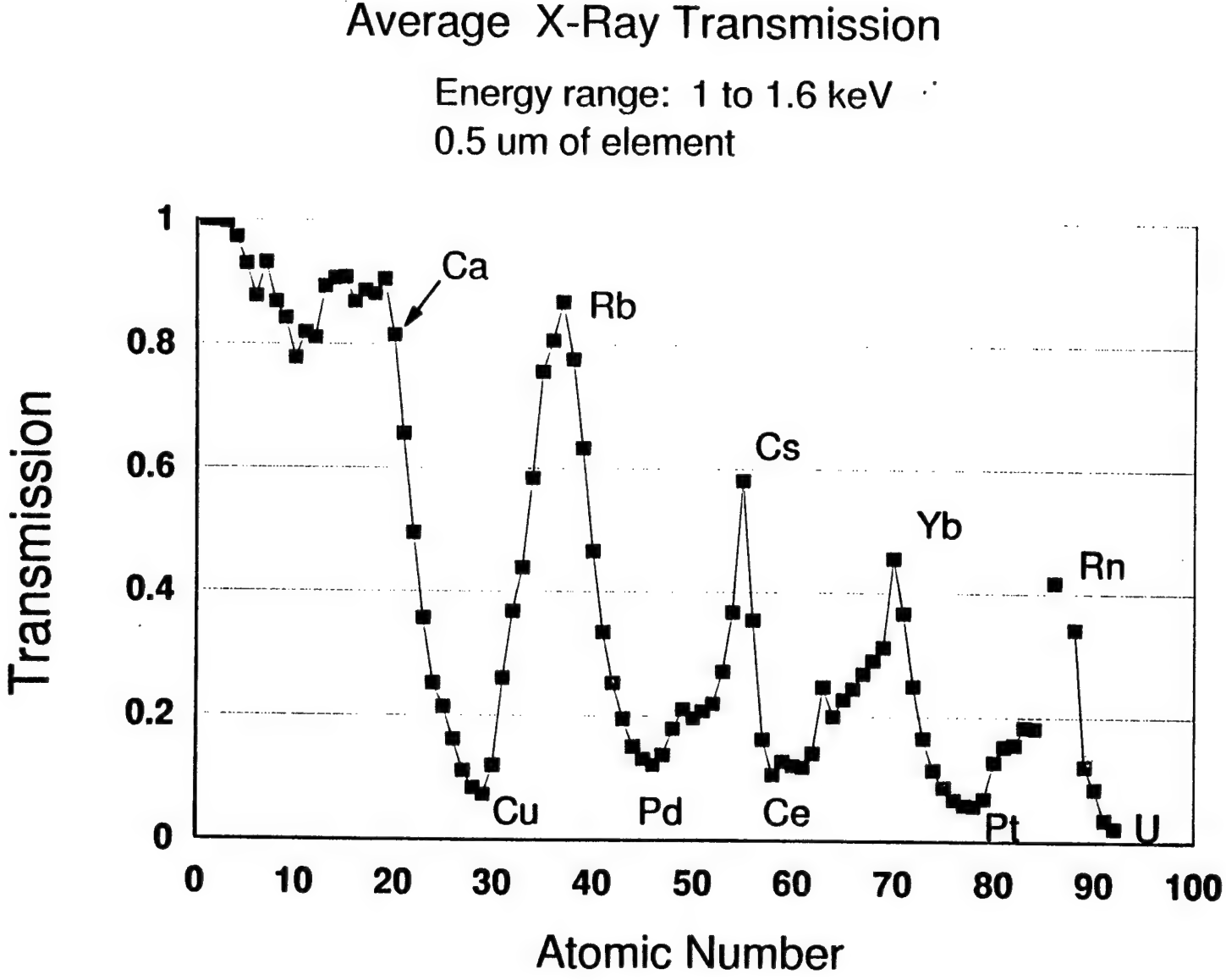

Average X-Ray Transmission
Energy range: 1 to 1.6 keV
0.5 um of element
Transmission
1
0.8
0.6
0.4
0.2
0
Ca
Rb
Cs
Yb
Rn
Cu
Pd
Ce
Pt
U
0
10
20
30
40
50
60
70
80
90
100
Atomic Number

Figure 10

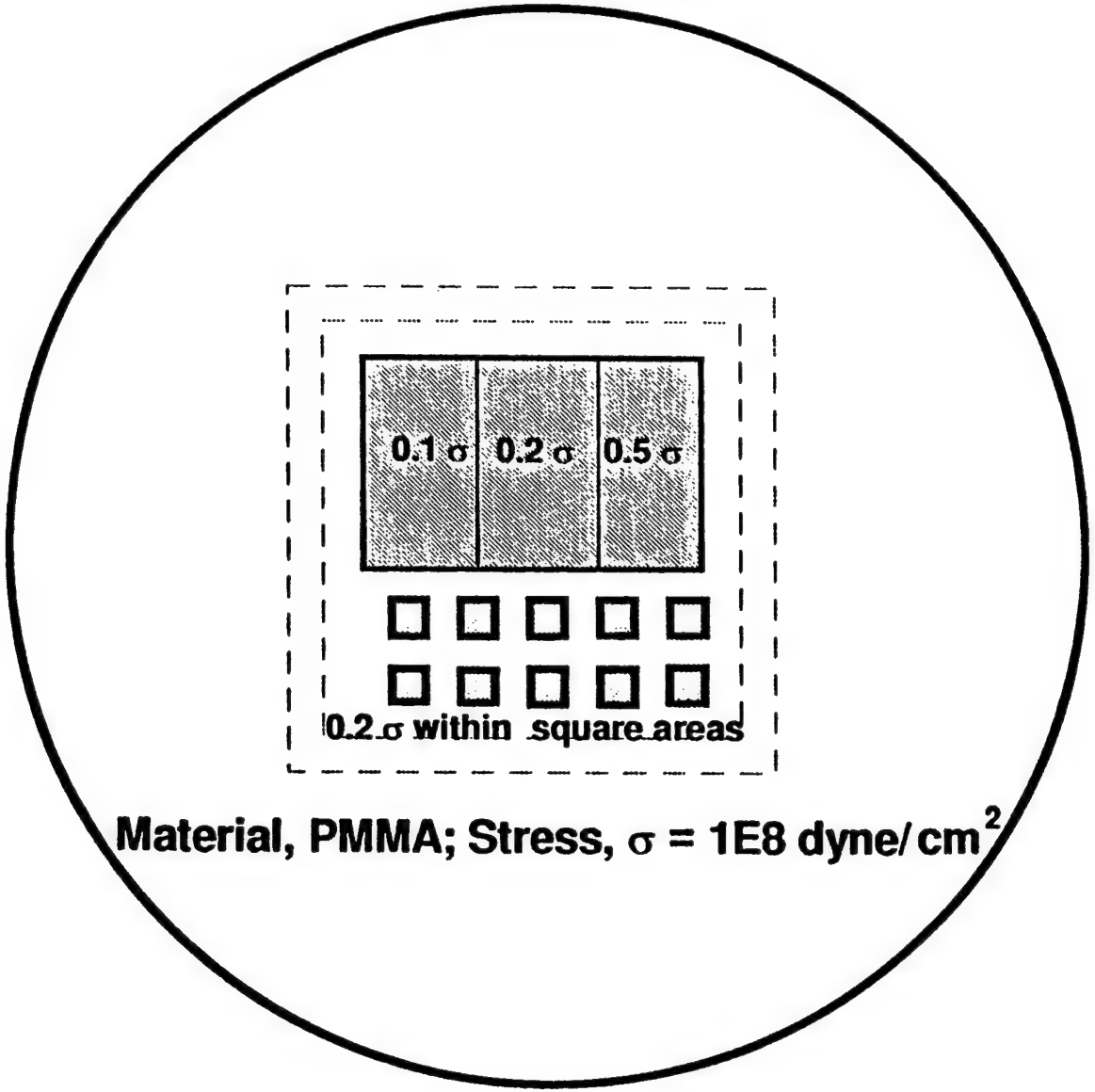

0.1 σ
0.2 σ
0.5 σ
0.2 σ within square areas
Material, PMMA; Stress, σ = 1E8 dyne/cm²

Figure 11

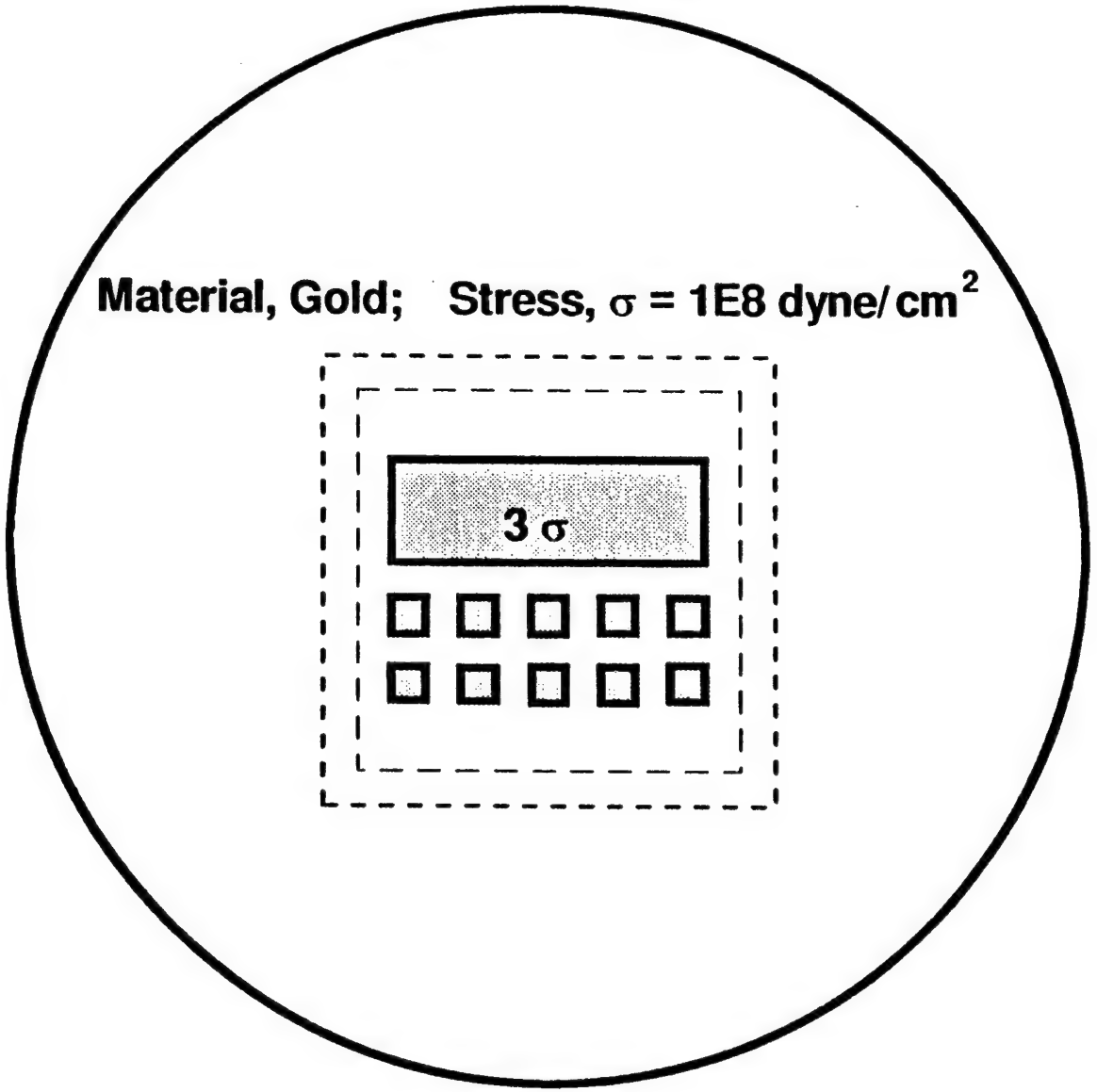


Figure 12

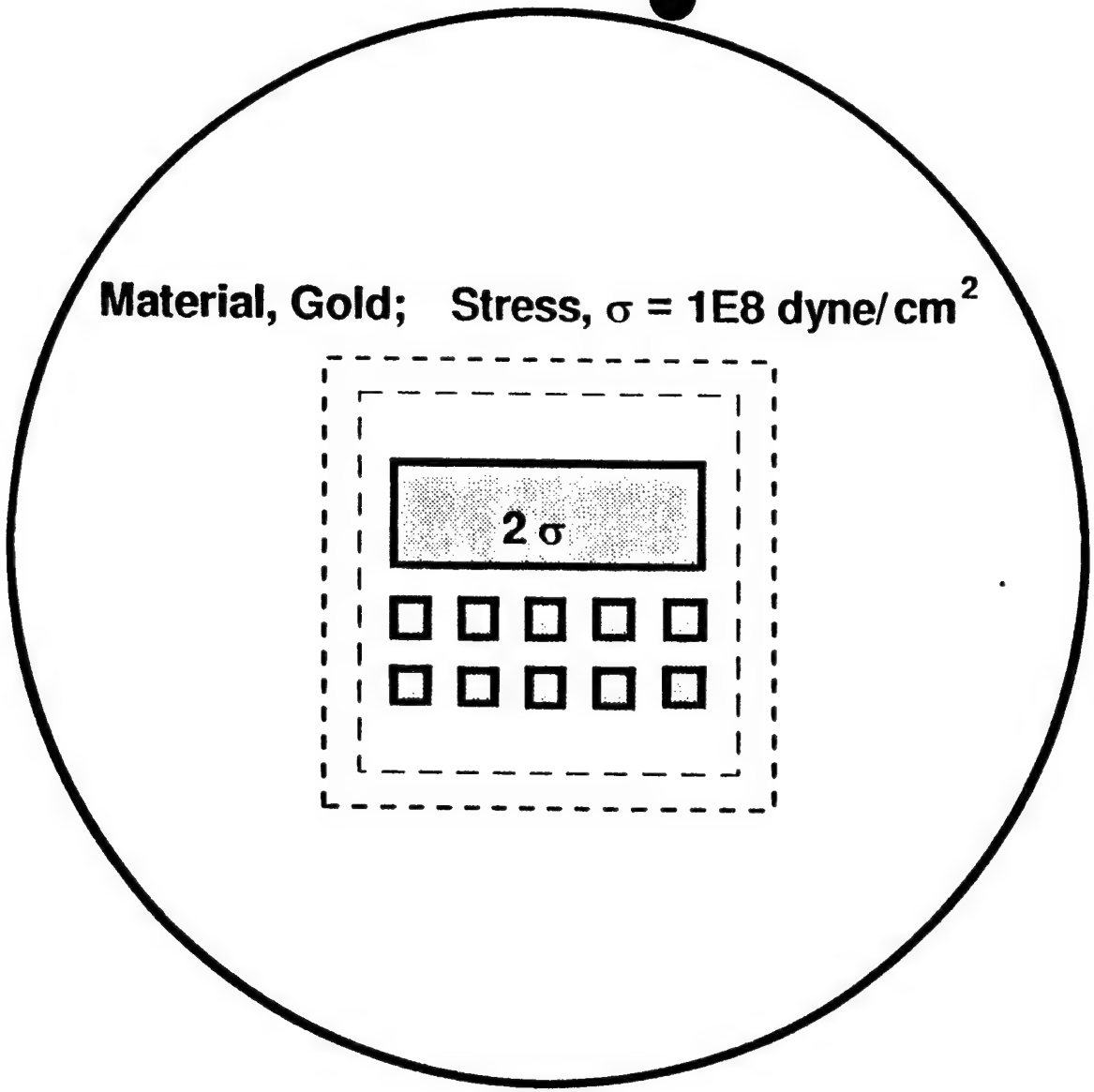


Figure 13

Appendix B. SVGL Summary

DALP X-Ray Aligner
Monthly Progress Report

SDRL A001

Period: May 24,1997 through October 31, 1997

Reference Contract Number N00019-94-C-0035

SVG SILICON VALLEY GROUP, INC.
Lithography Division

Table of Contents

1.0 Executive Summary

Program Status:

Beta Site Activities:

The major emphasis during this period was put toward completion of the Particle Detection System (PDS), installation of the Backup XRIS, support of small gap exposures and support of several Application exposures. Due to funding limitations during this period, the Aligner's throughput performance improvements were limited to completion of any "in process" throughput modifications. As directed,, no effort was expended on the Mask Cassette and Mask Handler Elevator activities during this period. This allowed the program to focus on the Particle Detection System, Backup XRIS, Support of Small Gap Operation, and Aligner Maintenance and Support activities.

Highlights for this period include:

- Integration of the Particle Detection System (PDS) into the Aligner.
- Completion of the Backup XRIS Integration and Test into the Aligner. This XRIS supports small gap operations of 15um under automated RUN conditions.
- Implementation of "in process" Throughput improvements resulting in Aligner Throughput times of 30 Wafer per Hour (based on 20 fields and one second exposure time).
- Completion of small gap characterization and Software improvements that supported gapping operational at 15um under automated RUN conditions.

Magnification Control:

Two different force configurations, balanced and unbalanced forces, were analyzed to see what arrangement yielded the lowest residual distortion when performing magnification control. Further analysis was performed to confirm the linearity of distortion with applied magnification correction.

SVGL prepared and presented materials on the MCO technique of mask mechanical deformation at a recent Technical Interchange Meeting (TIM). The customer hosted this meeting to show a status of work accomplished and to provide a discussion forum for currently known methods for providing magnification adjustment between the mask and wafer.

2.0 Beta Site Activities

2.2 Phase 2 Performance Improvements

2.2.1 Throughput Improvements

Throughput improvements have continued during this period but were limited to "in-process" upgrades in order to focus on higher priority tasks. Tasks completed include communication timing improvements, software upgrades at reduced Framing Blade move times and Mask alignment sequence improvements.

An investigation into the Communication delays between the Aligner & Beamline prompted SVGL to make a change in the Communication

protocol of the Beamline Software to match the internal communications in the Aligner environment. This Software upgrade resulted in Communication times ranging from 100 to 150 milliseconds verses previous times of 400 milliseconds prior to the upgrade. It is felt that further improvement can be made in an effort to meet the specification of 50 milliseconds. One potential effort would be to study making timing-oriented hardware upgrades on the Beamline computer and then make improvements based on results of that investigation.

A throughput performance demonstration in July resulted in measured Aligner Limited (based on 20 fields and one second exposure time) throughput of 30 Wafers per Hour. This data includes 4 field wafer global alignment on each wafer and 7 calibration alignments during a 25 wafer run. The data did not include wafers that required manual wafer intermediate alignment.

Throughput activities will resume when the Aligner Support Proposal, submitted in November of 1997, is accepted and authorized by the Customer. The Aligner Support Proposal includes Engineering activity that improves the Aligner Limited Throughput to 40 Wafers per Hour.

2.3 Particle Detection System

Progress on the Particle Detection System (PDS) focused on the subassembly build and integration of the electrical and mechanical subsystems. Tasks completed in this period include the assembly and test of the capacitance gage rectifier, assembly and test of the PDS mechanical subsystem, assembly and test of the PDS Bow, completion of the Hardware System Integration, completion of functional testing for all components, and the initial development and test of a wire-position calibration procedure.

The electrical subsystem activities included the build, debug and final test of the capacitance gage rectifier board, implementation of a Bow tuning tester, characterization of the PDS magnet signal, optimization of a Bow wiring technique, circuit board and harness documentation, servo optimization of PID parameters and supported PDS subassembly final test.

PDS servo testing included an open loop servo drive test that verified proper motor operation, amplifier and capacitance gage response as well as mechanical range and motion profile. Final subsystem servo testing was performed prior to system integration by connecting the PDS assembly externally to the Aligner while utilizing system harnessing and control hardware.

The Particle detection electronics that had been previously optimized on the test-wire fixture were optimized again with the real Bow assembly. Characterization tests were performed with 2 wire types, 0.6 mills and 2 mills. Although the 0.6 mill wire was more difficult to work with, it was chosen because it has better sensitivity resulting from its lower mass.

The mechanical subsystem activities focused on build and test of the PDS assembly. Final assembly was found to be more difficult than originally anticipated due to interactions between the flexure adjustment and the capacitance gage setting. Several adjustment iterations were required but ultimately all requirements were met.

The PDS-magnet gauss-reading was found to be below designed levels after the magnet was mounted in its holder assembly. Since

disassembly of the magnet from the holder could have damaged the magnet, it was decided to use it "as is" for initial integration and functional test. Meanwhile, a replacement magnet and holder assembly was built in parallel with integration tests. The cover material for the replacement magnet was changed from stainless steel to plastic due to potential magnetic flux reduction. Gauss meter readings of the replacement magnet were 4 times higher than that of the original magnet. This higher level is consistent with the design requirements. The magnet characterization and integration activity is expected to continue in the next reporting period.

PDS Integration activities included successful mechanical and electrical installation of all subsystems, functional verification of all components, servo optimization initial development and test of a wire-position calibration procedure.

A mechanical interference was encountered with an Off-Axis airpot bracket during the PDS installation. The airpot bracket was removed, reworked and reinstalled to eliminate the interference. This rework resulted in a minor shift of the image on the TV monitor during manual viewing. The final repair for the Off-Axis manual viewing has been deferred and the details are outlined in the Proposal submitted in November.

The Wafer Mapper was adjusted and calibrated and the Aligner was characterized with the PDS installed but turned off. The PDS servo was then characterized for bandwidth, stability, tracking and noise. Initial development and test of a wire position calibration procedure is in process and will continue in the next reporting period.

Software activities continued in this period. Tasks completed include the design, build and unit test of an initial RUN software version ready for integration that is scheduled to start in the next reporting period.

Plans for the next reporting period include:

- Integration and test of the replacement PDS magnet.
- Start of Software Integration tests.
- Continue development of the PDS Wire position Calibration.
- Continue the Build and Test of a second BOW assembly.
- Continue assembly and test of a portable BOW calibration test circuit.

2.5 Aligner Maintenance & Support

Wafer Load repeatability has been an issue in previous periods. An investigation performed this period yielded several sets of data demonstrating performance that meets specification. Subsequent exposures utilizing second level alignments also indicate specification-level performance in that the need for Manual Wafer Alignment has now become infrequent. We have concluded that the root cause of the earlier repeatability anomaly was an interference from the Wafer Robot hose, a condition that was corrected in a previous reporting period. Wafer Load Repeatability data will continue to be monitored during normal Preventative Maintenance periods to assure proper performance levels and continued adherence to specification.

Installation of the backup XRIS was completed in this period resulting in an XRIS capable of gapping operation down to 15micron. The XRIS was installed in June but required additional rework due to a mechanical interference in the mount that limited the rotational adjustment in the Aligner. The XRIS was mechanically reworked, cleaned and installed again in July. It was then characterized for in plane and out of plane positioning, Mask Alignment and Off-Axis signal levels and alignment performance. The backup XRIS was found to have performance comparable to the previous XRIS, while having improved out of plane characteristics in that the largest topography is estimated at 8 to 10 microns. The previous XRIS was found to have a large embedded particle of approximately 25 microns that limited the gapping operation of the system.

The investigation of an XRIS noise issue continued in this period. It was discovered that specific Masks when operated at small gaps would introduce large amounts of XRIS noise that would result in intermittent Mask alignment faults. A signal investigation discovered noise at 60Hz and 2khz. The source of this noise is now believed to be related to the large embedded particle in the original XRIS. This symptom has not been evident with the new XRIS. We speculate that the original XRIS was actually touching the Mask during small gap operations (25 to 30 microns) and thereby caused an impedance change in the detector circuit. We will continue to monitor performance but no other action is planned.

Support of "Small Gap (15 micron) under RUN" was initiated during this reporting period. Tasks completed include implementation of Software upgrades that check for high spots on the mask outside of the membrane area, tightening of the hard-coded wafer-protection plane value (peak above the wafer best fit plane) from 10 to 5 microns and implementation of post Wafer Leveling offsets that correct for systematic leveling errors. Several sets of gapping accuracy and stability data were also taken during this Period. The end result of this activity was several successful sets wafer exposures done at 15 micron gap under RUN software. Plans for next period include support of small gap application exposures and continued monitoring of gapping accuracy and stability data.

An issue with the Wafer Stage performance was found during this Period. Alignment repeatability data had become larger than normal. An investigation surfaced higher than normal noise levels on the monolithic Wafer Stage. A slight rubbing was also observed on one end of the X Substage. We found that the rubbing could be nearly eliminated by increasing the X Substage Airbearing pressure from 95 to 110 psi. The noise issue however is still under investigation and will continue in the next reporting Period.

Several Application exposures were completed in this Period including the start of 3300 wafer exposures for Mask Lifetime characterization. This test is expected to be completed in the next reporting period.

Plans for the next reporting period are to continue the Wafer Stage noise investigation and support continuing Application exposures.

2.6 Plans

Plans for November include:

- Continue the Particle Detection System Integration Activities
- Continue Maintenance and Support Activities

3.0 Magnification Control Activities

3.1 Status

A comparative analysis using a twelve force-actuator and sixteen force-actuator configuration has been performed using a NIST format mask. The system requirement of ±10.0 PPM for isotropic magnification resulted in 8.4 nm (3σ) residual distortion for the twelve actuator configuration. The sixteen actuator configuration resulted in 21.6 nm (3σ) residual distortion. Analysis shows that the twelve actuator configuration will be limited to ±6.0 PPM of magnification adjustment while the sixteen actuator configuration does allow for a adjustment up to ±10.0 PPM.

The analysis further showed that the largest vector distortions are at the membrane substrate boundary. A reduction of the overall distortion could be realized by providing for an edge exclusion zone in this area.

In June, SVGL prepared for and attended a Technical Interchange Meeting (TIM) on Magnification Correction for Proximity X-Ray Lithography at IBM - Burlington, Vermont. The meeting was held to discuss and evaluate various methods that have been under study by several participants for performing X-ray magnification correction. Presentations were given on several techniques including SVGL's Magnification Control Option program for mechanical deformation of the mask

The findings by SVGL thus far were shown to have more potential for performing magnification correction as compared to other techniques. Isotropic magnification adjustment of ±6 PPM can be achieved and residual distortions still meet the current DALP X-Ray Aligner overlay error budget.

The Magnification Control analysis in Phase 0 is complete. SVGL is now ready to proceed with Phase 1, Mag Control's proof-of-principal breadboard activity, as soon as funding is available.

3.2 Plans

Contingent upon initiation of Phase 1, plans for the next period will include:

- Perform FEA case studies on various membrane sizes.
- Further analyze silicon carbide membrane.
- Investigate potential out-of-plane effects while performing magnification control.

- Analyze pattern dependent distortions due to membrane stress change for absorber.
- Initiate mechanical design of force actuators based on current FEA preliminary conclusions.

4.0 Program Office

4.1 Funding

To date, SVGL has received $1,054,193 of contract authorized funding against CLIN 200 (Extended Support) and $263,000 against CLIN 201 (Magnification Control Option). As of 31 October 1997, $1,048,677 has been expended against CLIN 200 and $96,393 has been expended against CLIN 201.

4.2 Key activities in this reporting period

The program is in the process of preparing a proposal based on change order #6 to purchase order 286320. This proposal will extend the Aligner Support activity through December, 1998, and adds Small Gap activities. This proposal will be completed in early November. Additionally, a proposal for change order #5 to the Magnification Control Option was submitted on May 30, 1997. This proposal eliminated the hardware implementation option on the current Aligner, but added tasks including a system design study and a beamline design study.

The Program Office continues to maintain focus on software and hardware improvement activities that support Particle Detection system integration. An updated plan of Beta site activities is being used to track day-to-day activities.

Working reviews are being held at the Beta site on a weekly basis in lieu of the more formal monthly reviews at SVGL. This approach reduces preparation time and serves to maintain focus on day-to-day progress against plans.

4.3 Staffing Status

Additional staffing requirements will be filled from staff within SVGL's Advanced Programs department, and will be assigned on an as needed basis to assist with Engineering, Assembly and Design requirements.

4.4 Plans

Within the limits of available funding the Program office will, in conjunction with Lockheed Martin/IBM, continue to work to execute the updated Beta Site plan, and to assure coordination of Aligner, Beamline, and Process related integration activities.